3878 59737

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Date 2/5 Serial # 09/849,537 Priority Application Date 5/7/01

Your Name M. Lewis Examiner # _____

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In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need. 02-06-02 P12:27 IN

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a s archer for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?
Circle: (USPT) DWPI EPO Abs JPO Abs IBM TDB
Other: _____

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Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ___ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Novelty - Ball grid array package that has an improved heat spreader capability

Focus on claims 1-17

Staff Use Only

Searcher: Derrick Blaide
Searcher Phone: 306-0935
Searcher Location: TIC-EIC2800, CP1-9C18
Date Searcher Picked Up: 2/12/02
Date Completed: 2/13/02
Searcher Prep/Rev Time: 120
Online Time: 140

Type of Search
Structure (#) ___
Bibliographic ✓
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Fulltext ___
Patent Family ✓
Other ___

Vendors
STN ✓
Dialog ✓
Questel/Orbit ___
Lexis-Nexis ___
WWW/Internet ___
Other ___

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     FILE 'HCAPLUS' ENTERED AT 15:47:29 ON 08 FEB 2002
L1          2882 S BALL()GRID# OR BALLGRID? OR BGA OR BGAS OR PBGAS OR PBGA OR C
L2          1200 S (SOLDER OR SOLDERING OR SOLDERED OR BRAZ?)(2N)(BALL OR BALLS
L3         79308 S (HEAT? OR WARM? OR HOT# OR THERMOL? OR THERMAL? OR PREHEAT? O
L4          7003 S ((HIGH## OR HEIGHTEN? OR RAIS? OR INCREAS? OR ELEVAT?)(2N)(TE
L5         31095 S (CIRCUIT)(2N)(BOARD#) OR (SYSTEM?()BOARD#) OR MOTHERBOARD? OR
L6         64819 S SOLDER OR SOLDERING OR SOLDERED OR BRAZ?
L7        415074 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT#)) OR (MICRO)(
L8          3632 S (CONTACT? OR BONDING)(2N)(PAD OR PADS OR BUMP OR BUMPS)
L9          4992 S (WIRE OR WIRES OR LINE OR LINES)(2N)(BOND?)
L10         3403 S ((H01L-021/60 OR H01L-021/603 OR H01L-021/607))/IC
L11          515 S (CONDUCTIV?)(3N)(BUMP? OR PAD OR PADS)
L12         1251 S L1 AND (ENCLOS### OR HOUS### OR CASE# OR CONTAIN? OR ENCASE?
L13       461122 S HEAT(2N)SINK OR RING OR INTERPOSER OR STIFFENER
L14        30148 S L13 AND (L3 OR L4 OR 13)
L15            5 S L14 AND L2
L16            5 DUP REMOVE L15 (0 DUPLICATES REMOVED)
L17            2 S L14 AND L11
L18            5 S L14 AND L15
L19            5 S L18 OR L15
L20            7 S L14 AND L8
L21            5 S L16
L22            6 S L20 NOT (L16 OR L17)
L23          556 S L1 AND L7
L24       461122 S L13 AND (L3 OR L4 OR L13)
L25            5 S L16
L26           13 S L16-L22
L27           57 S L24 AND L2
L28           17 S L27 AND L5
L29           16 S L28 NOT L26
L30         6193 S L24 AND L7
L31           51 S L30 AND L8
L32           12 S L31 AND L9
L33           11 S L30 AND L11
L34           20 S (L32 OR L33) NOT L29
```

=> D BIB AB 1-5

L16 ANSWER 1 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:822820 HCAPLUS
TI Area array type semiconductor package and fabrication method
IN Song, Chi-jung
PA Hyundai Electronics Industries Co., Ltd., S. Korea
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6316837	B1	20011113	US 1998-200937	19981130
KR 1997-65912	A	19971204		

PI US 6316837 B1 20011113 US 1998-200937 19981130
PRAI KR 1997-65912 A 19971204

AB An area array type semiconductor package includes a plurality of conductive media, such as solder bumps or **solder balls**, attached to respective bond pads of a chip. The conductive media act as external output terminals. The chip is attached to a lead frame by a thermal conductive adhesive, and a predetermined area of the lead frame and the semiconductor chip are packaged with a molding resin. Leads of the lead frame are then trimmed and formed so that the lead frame, to which the semiconductor chip is adhered, acts as a **heat sink**. This allows the package to be used for a high-powered semiconductor device which **radiates** a **high temperature heat**. Also, because conductive media such as solder bumps or **solder balls** can be used to directly connect bond pads of the chip to conductive regions of a circuit board, a size of the semiconductor package can be minimized, the arrangement of the bonding pads on the chip can be easily planned, and electrical characteristics of the semiconductor package can be improved.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 2 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:930444 HCAPLUS
TI Heat resistance yes modification **heat sink** structure and its method ofapplication. [Machine Translation].
IN Ozawa, Tadashi
PA Nec Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001358269	A2	20011226	JP 2000-177715	20000614

PI JP 2001358269 A2 20011226 JP 2000-177715 20000614

AB [Machine Translation of Descriptors]. Improves the quality when working, also man-hour such as form modification and desorption of the **heat sink** offers decrease possible heat resistance yes modification **heat sink** structure. **Solder ball** 1 is arranged as one for connection of LS I2, the bottom plate the attaching screw 4 which installs 3 which installs the **heat sink** and the **heat sink** and **heat radiation** fin **distribution** facilities is done 5 and heat resistance conditioner 6 on back of LS I2. Heat resistance conditioner 6 is arranged on the center, is designed to be the structure which cuts off the wind for

cooling.

L16 ANSWER 3 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:213924 HCAPLUS
DN 131:6131
TI Improved adhesive performance through surface treatment
AU Gaynes, M. A.; Spalik, J. M.; Shaukatullah, H.
CS Microelectronics Division, IBM Corporation, Endicott, NY, USA
SO Prog. Durability Anal. Compos. Syst., Proc. Int. Conf., 3rd (1998), Meeting Date 1997, 241-246. Editor(s): Reifsnider, Kenneth L.; Dillard, David A.; Cardon, Albert H. Publisher: Balkema, Rotterdam, Neth. CODEN: 67KTAS
DT Conference
LA English
AB A surface mount tape ball grid array chip package [TBGA] uses flexible polyimide film to which elec. circuits were attached on both sides. To facilitate processing and handling, a picture frame metal **stiffener** is bonded to the film, with silicone adhesive. The opening in the **stiffener** defines the location wherein an integrated chip is placed and interconnected to the flexible circuit with thermo-compression bonds or flip-chip **solder balls**. With the chip backside exposed, heat transfer is enhanced by adhesively bonding a metal **heat spreader**. This **heat spreader** is also bonded to the **stiffener** and appears as a cover plate on the package. The adhesive bond to the cover plate, above the chip, degraded during the high heat exposure of solder reflow and temp. stress testing. Adhesion was improved significantly by oxidizing and hydrating the nickel plated surface of the cover plate. A silane coupler was also applied to the cover plate and further improved adhesion reliability.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 4 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:418127 HCAPLUS
DN 129:209769
TI Thermal performance of tape based ball grid array over molded packages
AU Edwards, Darvin; Hundt, Paul
CS Texas Instruments, Inc., Dallas, TX, 75265, USA
SO Annu. IEEE Semicond. Therm. Meas. Manage. Symp. (1998), 14th, 169-175 CODEN: ASTSFA; ISSN: 1065-2221
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB A near chip scale package based on area array technol. with a tape **interposer** is thermally evaluated using both computer models and measurement techniques. The package is described and compared to the thermal performance of QFP's with comparable phys. dimensions. The thermal performance of the package has been found to be highly dependent upon the arrangement of the **solder balls** on the **interposer** and on the die size. The impact of thermal **solder balls** and underfill is investigated, the contribution of a **heat spreader** is described, and **thermal** variation with material compn. is studied.

L16 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:677578 HCAPLUS
DN 125:313675
TI Flex tape ball grid array

AU Karnezos, Marcos; Goetz, Martin; Dong, Fred; Ciaschi, Andrew; Chidambaram, N.
CS ASAT Inc., Palo Alto, CA, 94303-4304, USA
SO Proc. - Electron. Compon. Technol. Conf. (1996), 46th, 1271-1277
CODEN: PETCES
DT Journal
LA English
AB Flex Tape Ball Grid Array (FTBGA) is a family of cavity down BGAs. The die, the flex tape and the **solder balls** are attached to the bottom side of a metallic **heat spreader** that acts as the **stiffener** and carrier of the package. The die is wire bonded to the tape traces and then encapsulated. The thermal and elec. performance and reliability are clearly superior to the alternative Plastic Ball Grid Arrays (PBGAs), the conventional plastic and thermally enhanced QFPs. The packages are constructed from materials that are well established in the industry. They are assembled using the same equipment, tools and processes as for the assembly of PBGAs.

=> D BIB AB 1-2

L17 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:747267 HCAPLUS
DN 135:281846
TI Method of preparing thermally conductive compounds by liquid metal bridged particle clusters
IN Misra, Sanjay
PA Bergquist Company, USA
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1143511	A2	20011010	EP 2001-303104	20010330
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6339120	B1	20020115	US 2000-543661	20000405
PRAI	US 2000-543661	A	20000405		
	US 2000-690994	A	20001017		

AB The present invention relates generally to an improved method and compn. for prepg. thermally conductive mech. compliant compds. for improving heat transfer from a heat generating semiconductor device to a heat dissipater such as a **heat sink** or **heat spreader** . More specifically, the present invention relates to the prepn. of improved formulations of highly thermally conductive polymer compds. such as a polymer liq. loaded or filled with percolating particulate clusters coated with a liq. metal and wherein the humidity resistance of the liq. metal is stabilized through the addn. of a hydrophobic alkyl functional silane, specifically octyltriethoxysilane. Such compds. are highly effective through liq. metal enhanced percolation, with the liq. metal having enhanced stability. The present invention involves a process for uniformly coating particulate solids with a liq. metal, and thereafter blending the coated particulate with a compn. comprising a blend of a liq. or fluid polymer and a hydrophobic alkyl functional silane, specifically octyltriethoxysilane to form a highly stable compliant pad with thermal vias therein. A thermally **conductive** mech. compliant **pad** of high stability including a quantity of Ga and/or In alloy liq. at temps. below .apprx.120.degree. and a B nitride particulate solid blended into the liq. metal alloy to form a paste. The paste is then combined with a quantity of a flowable plastic resin consisting of a blend of silicone oil and octyltriethoxysilane to form the mech. compliant pad, the compliant pad comprising from between .apprx.10% and 90% of metallic coated particulate, balance flowable plastic resin blend.

L17 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:89157 HCAPLUS
TI Method for coupling substrates and structure
IN Grupen-Shemansky, Melissa E.; Lin, Jong-Kai; Tessier, Theodore G.
PA Motorola, Inc., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	US 6022761	A	20000208	US 1996-654466	19960528

AB A method for connecting substrates includes using an adhesive **interposer** structure (11) to bond a semiconductor device (26) to a substrate (18). The adhesive **interposer** structure (11) includes a non-conductive adhesive laminant (12) and **conductive** adhesive **bumps** (13). The **conductive** adhesive **bumps** (13) provide a **conductive** path between **conductive bumps** (27) on the semiconductor device (26) and **conductive** metal **pads** (21) located on the substrate (18). In an alternative embodiment, a conductive adhesive material (34) is screen or stencil printed into vias (39) located on a printed circuit board (38) to form **conductive** adhesive **bumps** (33). A non-conductive adhesive (52) is then screen or stencil printed onto the printed circuit board (38) adjacent the **conductive** adhesive **bumps** (33). A semiconductor die is then connected to the structure.

L22 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:803755 HCAPLUS
DN 136:77770
TI Active circuits under wire **bonding** I/O **pads** in 0.**13** .mu.m eight-level Cu metal, FSG low-K inter-metal dielectric CMOS technology
AU Chou, Kuo-Yu; Chen, Ming-Jer
CS Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan
SO IEEE Electron Device Letters (2001), 22(10), 466-468
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Active circuits in terms of **ring** oscillator are moved to the place under the wire **bonding pads** in 0.**13** .mu.m full eight-level copper metal complementary metal-oxide-semiconductor process with fluorinated silicate glass low-k inter-metal dielec. The bond pad with the 12 K.ANG. thick aluminum metal film as a bonding mech. stress buffer layer is deposited on the topmost copper metal layer. No noticeable degrdns. in gate delay or cycle time of **ring** oscillator are detected in a variety of test structures subjected to bonding mech. stress and thermal cycling stress. This indicates that the underlying process technol. may be reliable and manufacturable in placing active circuits under the **bonding pads** and thereby the die area utility is recovered fully. More evidence is created from transmission line pulsing expts. as well as capacitive-coupling expts.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:771062 HCAPLUS
DN 135:297267
TI Power overlay chip scale flat-sided packages for discrete power devices
IN Fillion, Raymond Albert; Whitmore, Barry Scott; Korman, Charles Steven; Esser, Albert Andreas Maria
PA General Electric Company, USA
SO U.S., 33 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6306680	B1	20011023	US 1999-255412	19990222

PI US 6306680 B1 20011023 US 1999-255412 19990222
AB A power semiconductor device package includes at least one power semiconductor device mounted onto at least one elec. and thermally conductive spacer having an upper end surface bonded to a back surface of the device; a substrate of hardened substrate molding material surrounding the semiconductor device and the spacer except for an active major surface of the device and an lower end surface of the spacer, a dielec. film overlying the device active major surface and a top side of the substrate, the dielec. layer having a plurality of holes aligned with predetd. ones of the **contact pads**; a top side patterned metal layer on the dielec. film including portions extending into the holes elec. and thermally connected to **contact pads** of the device; and a backside metal layer on a substrate bottom side elec. and thermally connected to the spacer lower end surface. Optional through-post

structures can be employed to bring all elec. connections either to the top side of the device package or the bottom side. Optional **heat sinks** can be mounted to the top side, the bottom side, or both sides.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:391995 HCAPLUS
DN 134:360415
TI Process for producing a sealing and mechanical strength **ring** between a substrate and a chip hybridized by bumps on the substrate
IN Caillat, Patrice
PA Commissariat A L'energie Atomique, Fr.
SO U.S., 7 pp., Cont.-in-part of U.S. 553,495.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6238951	B1	20010529	US 1999-298696	19990423
PRAI FR 1993-6317	A	19930528		
WO 1994-FR620	A2	19940526		
US 1995-553495	B2	19951128		

AB Process for the prodn. of a sealing and mech. strength **ring** between a substrate and a chip hybridized by bumps on the substrate. The invention provides a process for producing an encapsulating **ring** (**13**) ensuring the sealing and mech. strength of a chip (1) hybridized by bumps on a substrate (5). More particularly, contemporaneously with the prodn. of the hybridization bumps (9) on the lower face (1a) of the chip or the substrate by a 1st meltable material, a sealing and mech. strength **ring** is formed by depositing on the substrate or lower face of the electronic component a **ring** (**13**) of a 2nd meltable material. The lower face of the chip then is placed on the substrate so as to produce the connections between said chip and said substrate by the 1st meltable material, and the thus formed assembly is heated to a temp. at least equal to the highest m.p. of the 1st and 2nd meltable materials, in order simultaneously to produce the hybridization bumps of the 1st material and the sealing **ring** of the 2nd material. The **ring** is sized to have a height (h) and a width (d) in accordance with the following equation: d > (10-2Dh)/(h-.alpha.) in which .alpha. is a shape coeff. factor and D is the largest dimension of the electronic component.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:599355 HCAPLUS
TI Integrated circuit package having a **stiffener** dimensioned to receive heat transferred laterally from the integrated circuit
IN Kutlu, Zafer S.
PA Lsi Logic Corporation, USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	US 6111313	A	20000829	US 1998-5491	19980112

AB A system and method are presented for forming a grid array device package around an integrated circuit (i.e., chip). The device package includes a substrate, a **stiffener**, a **heat spreader**, and an optional **heat sink**. The chip includes multiple I/O pads arranged upon an underside surface. The substrate includes a first set of **bonding pads** on an upper surface configured to vertically align with the I/O pads. The chip is connected to the first set of **bonding pads** using the C4 method. The **stiffener**, a rigid member able to retain its shape during C4 heating, may be attached to the upper surface of the substrate prior to the C4 process, helping the substrate maintain its planarity during and after the C4 process. The **stiffener** has an opening dimensioned to receive the chip and exposing the first set of **bonding pads**. Following the C4 process, a first space between the underside surface of the chip and the upper surface of the substrate is filled with an underfill material. A second space between the side surfaces of the chip and side walls of the opening in the **stiffener** is filled with an underfill material or a thermal interface material. The underfill or interface material filling the second space provides additional thermal paths for heat energy to flow from the chip to the ambient. The **heat spreader** is attached to upper surfaces of the **stiffener** and the chip, and the **heat sink** is optionally attached to the upper surface of the **heat spreader**.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:483826 HCAPLUS
TI Assembly for dissipating heat from a stacked semiconductor package
IN Lee, Won Sang
PA Lg Electronics, Inc., S. Korea
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6091142	A	20000718	US 1997-991239	19971216
PRAI	KR 1996-66223	A	19961216		

AB A stacked semiconductor package and a method for assembling the same are disclosed, the stacked semiconductor package including a semiconductor chip having a plurality of wire **bonding pads** thereon; leads formed in a direction to electrically connect with the wire **bonding pads**; a **heat sink** connected to the predetermined wire **bonding pad** to **radiate** out **heat** of the semiconductor chip; and an epoxy supporting and protecting the semiconductor chip, the leads, and the **heat sink**.

=> D BIB AB 1-5

L29 ANSWER 1 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:848550 HCAPLUS
TI Grid array package with reduced power and ground impedance under high frequency
IN Lee, Chun-ho
PA Taiwan
SO U.S. Pat. Appl. Publ.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001042914	A1	20011122	US 2001-858651	20010517
TW 2000-89109870	A	20000522		

PI
PRAI
AB A grid array (GA) package for holding a die therein, the die accessing its operational power from a printed **circuit board** through the GA package, the GA package comprises a substrate with a die cavity. A first conductive layer is provided on a top surface of the substrate, a **ring** is provided surrounding the die cavity whereby the die electrically connects the first conductive layer via the **ring**. A second conductive layer is provided on a bottom surface of the substrate. A plurality of vias are provided within the substrate to connect the first conductive layer with the second conductive layer. A plurality of **solder balls** are provided on the bottom surface of the second conductive layer to connect the second conductive layer with the printed **circuit board**. Individual **solder ball** is horizontally closer to the die cavity in comparison with at least one associated via. Therefore when power transfers from individual **solder ball** through the second conductive layer, at least one associated via, the first conductive layer, and the **ring**, finally to the die. The direction of current that flow through the second conductive layer is opposite to the direction of current that flow through the first conductive layer, so as that the magnetic field produced by the current flow through the second conductive layer cancels out the magnetic field produced by the current flow through the first conductive layer, to decrease the power and ground impedance of the substrate.

L29 ANSWER 2 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:681611 HCAPLUS
TI **Solder** thieving **pad** for wave **soldered** through-hole components
IN Lin, Kon M.; Groves, Quentin D.; Robinson, Albert W.
PA Lucent Technologies, Inc., USA
SO U.S., 18 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6292372	B1	20010918	US 1999-353386	19990715

PI
AB An improved robber or **solder** thieving **pad**, parallelogram shaped, significantly reduces solder bridging in wave soldered multi leaded through hole or surface mounted components in a printed **circuit board** for different wave settings.

The component leads are either parallel or perpendicular to the solder wave during the soldering process. In one embodiment, the parallelogram shaped **solder** thieving **pad** is disposed contiguous or adjacent to the through hole. In another embodiment, the parallelogram shaped **solder** thieving **pad** is spaced from a thin annular **ring** surrounding the through-hole. In still another embodiment, the pad may be linked to the **ring** by a thin connecting bridge. Dimensions of the **solder** thieving **pad** vary according to the component lead size, spacing, and number of rows. The design of the pad takes into account the total molten solder volume held in a solder joint and balances the weight of the solder volume, the dynamic solder flow in the wave; and the solder surface tension for improving the drainage behavior of the solder to inhibit solder bridging of the component leads.

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 3 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:627199 HCAPLUS
DN 135:173793
TI Method of forming an integrated circuit package at a wafer level
IN Lam, Ken M.
PA Atmel Corp., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6281046	B1	20010828	US 2000-558396	20000425

AB A method is presented for forming an integrated circuit package at the wafer level. The integrated circuit package occupies a min. amt. of space on an end-use printed **circuit board**. Solder bumps, or conductive adhesive, is deposited on the metalized wire bond pads on the top surface of a Si wafer. An underfill-flux material is deposited over the wafer and the solder bumps. A pre-fabricated **interposer** substrate, made of metal circuitry and a dielec. base, has a plurality of metalized through-holes which are aligned with the solder bumps. The wafer/**interposer** assembly is reflowed, or cured, to form the elec. connection between the circuitry on the **interposer** layer and the circuitry on the wafer. **Solder balls** are then placed on the metal pad openings on the **interposer** substrate and are reflowed to form a wafer-level BGA structure. The wafer-level BGA structure is then cut into individual BGA chip packages.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 4 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:597605 HCAPLUS
DN 135:161098
TI BGA (ball grid array) or CSP (chip scale package) area array IC chip
IN Sakata, Ikuaki
PA Yasukawa Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001223294	A2	20010817	JP 2000-32089	20000209

AB The invention relates to an area array semiconductor device, i.e., BGA (ball grid array) or CSP (chip scale package) area array IC chips, wherein the **solder balls** on the **interposer** are mated with cream solder array of the **circuit board**.

L29 ANSWER 5 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:423717 HCAPLUS
TI Method for wire bonding a chip to a substrate with recessed bond pads and devices formed
IN Chen, Tsung-chieh; Chen, Chun-liang; Liao, Kuang-ho
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6245598	B1	20010612	US 1999-305945	19990506

AB A method for forming chip scale packages and devices formed by utilizing a wire bonding technique and an **interposer** board which has recessed peripheral regions are disclosed. In the method, an IC die is bonded on its active surface to an **interposer** which is constructed with a recessed peripheral regions equipped with interconnections such that shorter bond wires may be run between the IC die and the **interposer**. The **interposer** is further equipped, in a top planar surface, with a plurality of interconnections for the subsequently forming of **solder balls** for connecting to an outside circuit such as a printed **circuit board**. The present invention novel method further provides the benefit that the shorter wire bonds formed alleviate the wire sweep problem normally occurs in the plastic encapsulation process for such a package.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> D BIB AB 6-16

L29 ANSWER 6 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:222098 HCAPLUS
TI Microelectronic component with rigid **interposer**
IN Bellaar, Pieter H.; Distefano, Thomas H.; Fjelstad, Joseph; Pickett, Christopher M.; Smith, John W.
PA Tessera, Inc., USA
SO U.S., 9 pp., Division of Ser. No. US 1997-978082, filed on 25 Nov 1997
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6208025	B1	20010327	US 1999-413410	19991006
	US 2001048591	A1	20011206	US 2001-771412	20010126
PRAI	US 1997-978082	A3	19971125		
	US 1999-413410	A2	19991006		

US 2000-178125 P 20000126

AB A microelectronic component for mounting a rigid substrate, such as a hybrid circuit to a rigid support substrate, such as a printed **circuit board**. The microelectronic component includes a rigid **interposer** which may have a chip mounted on its first surface; a pattern of contacts on the rigid **interposer**; a flexible **interposer** overlying the second surface of the rigid **interposer**; a pattern of terminals on the flexible **interposer**; flexible leads; and **solder** coated copper **balls** mounted on the flexible **interposer**. The microelectronic component may have a socket assembly mounted on the first surface of the rigid **interposer**. The microelectronic component may be mounted on a rigid support substrate.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 7 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:62930 HCAPLUS
DN 134:140331
TI Fabrication of lead-wired **circuit boards** for mounting semiconductor devices
IN Miyazawa, Hiroaki; Kawai, Kenzaburo; Umeda, Kazuo
PA Dainippon Printing Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001024141	A2	20010126	JP 1999-198737	19990713

AB The title fabrication involves (1) forming an etching stopper on the front side of a metal substrate and electrodepositing a circuit layer for formation of lead wires, (2) coating a pos. photochem. polyimide varnish over the plated circuit layer on the front and on the rear sides of the substrate and drying for semi-curing, (3) patterning the polyimide layer as an insulator layer by photolithog. to give openings for exposing portions of the lead wirings, (4) electrodepositing over the insulator layer as a mask to give external contact terminals on the lead wires, (5) patterning the polyimide layer on the rear side of the substrate by photolithog. so as to remove the layer from areas corresponded to the lead forming regions on the front side, (6) selective etching over the patterned polyimide layer as a mask to give a peripheral **ring** on the rear side of the substrate, and (7) etching the etching stopper layer to isolate the leads and hanging peripheral edge. The pos. photochem. polyimide varnish may contains diazonaphthoquinone or its derivs. and a solvent-sol. polyimide. The use of the specific photochem. polyimide varnish makes possible in repeated photolithog. patterning over the single insulative mask and eliminating an etching for a resist mask formation on the rear side as well as for a **solder ball** formation.

L29 ANSWER 8 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:24687 HCAPLUS
DN 134:230535
TI Modified plugging design for through-hole via-in-pad printed **circuit boards**
AU Anon.
CS UK
SO Res. Discl. (2000), 440(Dec.), P2093-P2094 (No. 40070)

CODEN: RSDSBB; ISSN: 0374-4353
PB Kenneth Mason Publications Ltd.
DT Journal; Patent
LA English

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI RD 400070		19970810		
PRAI RD 1997-400070		19970810		

AB To minimize the solder waste from the via in pad to the through hole, a modification of the printed **circuit board** (PCB) soldermask plugging process is presented. Cross sections of the conventional PCB process and its modification are depicted and dicussed. The plugging operation now no longer blocks the flow of gas or liqs. from one side to the other. The trapping of gas bubbles in the **solder ball** called voiding can have a detrimental effect for the component by causing bridges between the **solder balls**. This voiding is eliminated in the **solder balls** for the through-hole via-in-pad boards. Furthermore, the via remains open after the assembly process allowing to remove the heat by both conduction and convection without a **heat sink** being necessary.

L29 ANSWER 9 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:22796 HCAPLUS
DN 134:201009
TI Effects of lead bonding process on reliability of chip scale package
AU Lee, Yeong J.; Eyre, Matthew W.
CS Electronic Packaging Materials Development, Dow Corning Corporation, Midland, MI, 48686-994, USA
SO Proc. - Electron. Compon. Technol. Conf. (2000), 50th, 1392-1397
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB An integrated circuit (IC) package has become smaller and its profile becomes lower as new chip scale packaging (CSP) designs have been introduced. A new design of packages demands new materials and optimization of manufg. processes to enhance reliability of the package. A compliant layer in Tessera's .mu.-BGA package is a crucial component to increase **solder ball** reliability in the board level assembly. The compliant layer can reduce damage to the **solder balls**, which is induced by mismatch of the coeff. of thermal expansion (CTE) between Si die and the printed **circuit board** (PCB). Silicone elastomer is one of the best candidate for the compliant layer due to its low modulus and low moisture absorption. While the **solder ball** reliability in the .mu.-BGA package is significantly improved due to its unique design and optimal materials set, fatigue damage can be imposed on beam leads inside of the package during thermal cycling. To reduce the damage in the package, an optimal lead (or beam lead) bonding process becomes crit. for flex circuit **interposer** type of CSP designs including .mu.-BGA. Three dimensional (3-D) Finite Element Anal. (FEA) of the lead bonding and subsequent thermal cycling, is conducted to show effects of designs of the lead (dimensions and shapes) as well as the lead bonding process parameters. Several different loci of a bond tool motion are numerically simulated to det. optimal lead bonding parameters based on the calcd. damage accumulated in the deformed shape of leads during the lead bonding process followed by the thermal cyclings.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 10 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:906005 HCAPLUS
TI Package socket system
IN Lin, Nick; Lin, Cheng-hung
PA Hon Hai Precision Ind. Co., Ltd., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6164981	A	20001226	US 1999-291791	19990414
PRAI TW 1998-87214313	U	19980831		

AB A package socket system includes a positioning frame positioned on a **circuit board**. The positioning frame has an interior space defined between four side walls for receiving and accommodating a BGA socket that retains an array of contacts therein. The contacts have a lower ball end in contact engagement with and supported on conductive pads of the **circuit board**. A BGA package having an array of **solder balls** is received in the positioning frame and supported on the socket with the **solder balls** received in flared upper ends of the contacts of the socket. A **heat sink** has a flat base supported on the positioning frame and secured to the substrate to establish a firm contact engagement with the package thereby securely maintaining the package and the socket in position on the substrate. The positioning frame has a chamfered section and the socket and the package each have a corresponding chamfered corner for positioning purposes.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 11 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:814774 HCAPLUS
DN 133:358177
TI Method for manufacturing a printed **circuit board** with integrated **heat sink** for semiconductor package
IN Juskey, Frank J.; McMillan, John R.; Huemoeller, Ronald P.
PA Amkor Technology, Inc., USA
SO PCT Int. Appl., 24 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2000069239	A1	20001116	WO 2000-US13041	20000511
W: CA, JP, KR, SG				
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
US 6337228	B1	20020108	US 1999-310660	19990512
PRAI US 1999-310660	A	19990512		

AB A low-cost printed **circuit board** (10) for a semiconductor package having the footprint of a ball grid array package has an integral **heat sink** (20), or slug, for the mounting of one or more semiconductor chips, capable of efficiently conducting away at least five watts from the package in typical applications. It is made by forming an opening (16) through a sheet, or

substrate (14), of B-stage epoxy/fiberglass composite, or pre-preg, then inserting a slug (20) of a thermally conductive material having the same size and shape as the opening into the opening. The slug-contg. composite is sandwiched between two thin layers (30) of a conductive metal, preferably Cu, and the resulting sandwich (10) is simultaneously pressed and heated between the platen (12) of a heated press. The heat and pressure forces the resin to the surface of the composite (10) and into the space between the slug (20) and the walls of the composite, where it solidifies, bonding the edges of the slug (20) to the substrate (14) within the opening and adhering the conductive layers (30) to the upper and lower surfaces of the substrate (14). The resulting laminate (10) can thereafter be processed as a convention printed **circuit board** to incorporate conventional **circuit board** features, e.g., circuit traces, wire bonding **pads**, **solder ball** mounting lands, and via holes.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 12 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:641062 HCAPLUS
DN 133:316292
TI Impact properties of PBGA assemblies reflowed in nitrogen ambient and compressed air
AU Wu, Y. P.; Chan, Yan C.
CS Department of Electronic Engineering, City University of Hong Kong, Kowloon, Hong Kong
SO IEEE Trans. Adv. Packag. (2000), 23(3), 421-425
CODEN: ITAPFZ; ISSN: 1521-3323
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB In this paper, the solder joint brittleness of plastic ball grid array (PBGA) assemblies has been studied by means of impact testing. The results show that the max. impact force and the impact energy for PBGA assemblies reflowed in nitrogen ambient is higher than for those reflowed in compressed air. Redn. of the oxygen content from 1000 ppm to 50 ppm reduces the initiation energy of impact. The impact fractured surfaces occur between the printed **circuit board** (PCB) **pads** and **solder** joints, i.e., in the brittle intermetallics region. The pores and impurities are mainly distributed within a **ring** at the perimeter of the interface, with greater d. at the edges than at the center. Reflow in a nitrogen ambient reduces the defect d., with redn. in oxygen content farther reducing the d. Impact cracks begin from the defects of the Cu/solder interface, and propagate along the intermetallics.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 13 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:636235 HCAPLUS
DN 133:216532
TI Fabrication of semiconductor component with external contact polymer support
IN Farnworth, Warren M.; Wood, Alan G.
PA Micron Technology, Inc., USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6118179	A	20000912	US 1999-384783	19990827
	US 6180504	B1	20010130	US 1999-440380	19991115
PRAI	US 1999-384783	A3	19990827		

AB A semiconductor component includes a substrate, bonding pads on the substrate, and external contacts bonded to the bonding pads. Exemplary external contacts include **solder balls**, **solder** bumps, **solder** columns, TAB bumps and stud bumps. Preferably the external contacts are arranged in a dense array, such as a ball grid array (BGA), or fine ball grid array (FBGA). The component also includes a polymer support member configured to strengthen the external contacts, absorb forces applied to the external contacts, and prevent sepn. of the external contacts from the bonding pads. In a first embodiment, the polymer support member comprises a cured polymer layer on the substrate, which encompasses the base portions of the external contacts. In a second embodiment, the polymer support member comprises support **rings** which encompass the base portions of the external contacts. In either embodiment the polymer support member transfers forces applied to the external contacts away from the interface with the bonding pads, and into the center of the contacts.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 14 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:618577 HCAPLUS
TI **Solder ball** grid array carrier package with **heat sink**
IN Oh, Sang Eon
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 6 pp., Cont. of Ser. No. US 1996-755098, filed on 25 Nov 1996, now abandoned
CODEN: USXXAM
DT Patent
LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5959356	A	19990928	US 1997-953381	19971017
PRAI	KR 1995-43760		19951125		
	US 1996-755098		19961125		

AB A **solder ball** grid array carrier package has a **circuit board** with conductive wirings and a plurality of through holes. At least one semiconductor chip is mounted on an upper surface of the **circuit board** and bonding wires electrically connect the chip to the conductive wirings. A plurality of **solder balls** are electrically connected to the conductive wirings, with the **solder balls** being adhered to a lower surface of the **circuit board**. A **heat sink** is also adhered to the lower surface of the **circuit board**. The **heat sink** is in direct contact with the through holes of the **circuit board**, with the through holes allowing for heat dissipation.

L29 ANSWER 15 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:81607 HCAPLUS
DN 130:147311
TI A metallic coating used for manufacturing and assembling electronic

components such as interconnects
IN Kivilahti, Jorma
PA Finland
SO PCT Int. Appl., 15 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 9903632	A1	19990128	WO 1998-FI594	19980714

W: CN, JP, US
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE

PRAI FI 1997-2982 19970714

AB The invention relates to a metallic coating, which can be used, for example, for manufg. electronic components and for interconnecting irreversibly the components into various substrates by employing either low temp. or high temp. solders. It is characteristic for the invention that the coating enables one to interconnect electronic components fluxlessly. The invention relates esp. to the interconnection technique which was used for example for interconnecting bare chips to the **interposer** of surface mount package or directly on substrate like printed wiring board or interconnecting surface mount package on printing wiring board. The object of the present invention is in particular the interconnection technique in which the electrolytically deposited solder bumps on elec. contact pads are replaced with self-contained **solder balls** which make the alloys selection of the bumps more versatile, simpler and cheaper to accomplish. It is in accordance with the present invention to coat **solder balls** and Sn or tin-alloy precoated contact surfaces with the Bi layer of appropriate thickness. It is also in accordance with the present invention to place Bi-coated solder particles to contact areas mixed in org. solvent as a paste or as an anisotropically conducted adhesive.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 16 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:218684 HCAPLUS
DN 126:219542
TI Ball grid array electronic package
IN Robinson, Peter W.; Mahulikar, Deepak; Hoffman, Paul R.
PA Olin Corp., USA
SO PCT Int. Appl., 24 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 9704629	A1	19970206	WO 1996-US11461	19960709

W: AL, AM, AT, AU, AZ, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG
RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG

AU 9664500	A1	19970218	AU 1996-64500	19960709
EP 882384	A1	19981209	EP 1996-923727	19960709

R: DE, GB

PRAI US 1995-502662 19950714
WO 1996-US11461 19960709

AB The bending of a ball grid array electronic package having a metallic base is reduced, minimizing stresses applied to the innermost row of **solder balls**, when the package base is cyclically heated and cooled. Reducing the stresses applied to the **solder balls** increases the no. of thermal cycles before **solder ball** fracture causes device failure. Among the means disclosed to reduce the bending moment are a bimetallic composite base, an integral **stiffener**, a centrally disposed cover bonded to an external structure, and a package base with a stress-accommodating depressed portion.

=> D BIB AB 1-20

L34 ANSWER 1 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:10946 HCAPLUS
DN 136:94469
TI Ball-grid array package on semiconductor **chips** for increased heat dissipation
IN Huang, Chien-Ping; Her, Tzong-Dar
PA Taiwan
SO U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002000656	A1	20020103	US 1999-451135	19991130

AB Thermal-dissipation substrates have the 1st surface and the 2nd surface, and elec. insulating interlayer and top Cu foil are built up sequentially on the 2nd surface. The Cu foil is patterned to form multiple conducting wire lines, and then a solder resist coating is applied on the surfaces of both the conducting wire lines and the insulating interlayer. A part of the conducting Cu surface is exposed to form multiple bonding tips and multiple ball pads. An aperture is formed at the center, to penetrate thermal dissipation substrate and the insulating layer. A semiconductor **chip** has its active surface bonded to the 1st surface, and has multiple **bonding wires** passing through the aperture for elec. connection to the **bonding pads**. The finished **chip** with the **bonding wires** and tips is encapsulated, and solder balls are placed on the resp. ball pads.

L34 ANSWER 2 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:861538 HCAPLUS
TI Semiconductor package having **heat sink** at the outer surface
IN Huang, Chien-ping
PA Taiwan
SO U.S. Pat. Appl. Publ.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001045644	A1	20011129	US 2000-482425	20000113

AB A semiconductor package having **heat sink** at the outer surface is constructed on a lead frame. The package comprises a **chip**, a **die** pad, a plurality of leads, a plurality of **bonding wires**, and a molding compound. The **die** pad has a first surface and a second surface, and the **chip** has its active surface bonded to the first surface of the **die** pad. The area of the **die** pad is smaller than the area of the **chip** in order to expose the **bonding pads** on the active surface of the **chip**. The leads having an inner lead portions and an outer lead portions are disposed at the periphery of the **die** pad, and the inner lead portions are electrically connected to the **bonding pads** by a plurality of **bonding wires**. The molding compound encapsulates the **chip**, the

die pad, the inner lead portions of the leads, and the **bonding wires**. The second surface of the **die** pad is exposed on the top surface of the package structure while the outer lead portion of the leads is exposed at the side edge of the package structure.

L34 ANSWER 3 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:803755 HCAPLUS
DN 136:77770
TI Active circuits under **wire bonding** I/O **pads** in 0.13 .mu.m eight-level Cu metal, FSG low-K inter-metal dielectric CMOS technology
AU Chou, Kuo-Yu; Chen, Ming-Jer
CS Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan
SO IEEE Electron Device Letters (2001), 22(10), 466-468
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Active circuits in terms of **ring** oscillator are moved to the place under the **wire bonding pads** in 0.13 .mu.m full eight-level copper metal complementary metal-oxide-semiconductor process with fluorinated silicate glass low-k inter-metal dielec. The bond pad with the 12 K.ANG. thick aluminum metal film as a bonding mech. stress buffer layer is deposited on the topmost copper metal layer. No noticeable degrdns. in gate delay or cycle time of **ring** oscillator are detected in a variety of test structures subjected to bonding mech. stress and thermal cycling stress. This indicates that the underlying process technol. may be reliable and manufacturable in placing active circuits under the **bonding pads** and thereby the **die** area utility is recovered fully. More evidence is created from transmission line pulsing expts. as well as capacitive-coupling expts.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 4 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:778994 HCAPLUS
TI **Chip** package and method of making and testing the same
IN Wang, Peter; Huang, Yu-wen
PA Ang Technologies Inc., USA
SO U.S. Pat. Appl. Publ.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001033017	A1	20011025	US 2001-766081	20010119
PRAI	US 2000-177129	P	20000120		

AB A flip-**chip IC** package configured for ease of testing comprises a substrate and a plurality of **stiffener** walls, each **stiffener** wall carrying an **IC**, wherein the **stiffener** walls and **ICs** are fixed to the substrate with electrical continuity being established between the substrate and the **stiffener** walls and **IC**'s through **conductive bumps** (solder **bumps** or **conductive** epoxy **bumps**). The substrate and the **stiffener** walls include

test points on their surfaces, and also include printed electrical circuitry connecting the test points and the **conductive bumps**. Some of the printed electrical circuitry is arranged to establish paths between test points which facilitate testing of **conductivity** through the **conductive bumps**, and which facilitate functional testing of the **ICs**.

L34 ANSWER 5 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:385971 HCAPLUS
TI Reinforcement of lead bonding in **microelectronics** packages
IN Jiang, Tongbi
PA Micron Technology, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6239489	B1	20010529	US 1999-365599	19990730
	US 2001028116	A1	20011011	US 2001-859323	20010516
PRAI	US 1999-365599	A3	19990730		

AB The present invention is directed toward an apparatus and method of reinforcement of lead bonding in **microelectronics** packages. In one embodiment, a **microelectronics** package includes a **microelectronics** device having a bond **pad**, a **conductive** lead having a first end bonded to the bond pad to form a lead bond, an encapsulating material at least partially disposed about the conductive lead, and a reinforcement portion at least partially disposed about the lead bond and at least partially coupling the first end to the bond pad. The reinforcement portion has a greater modulus of elasticity and/or a greater bond strength than the encapsulating material. During thermal cycling of the **microelectronics** package, bond liftoff due to CTE mismatch is prevented by the reinforcement portion. The reinforcement portion may include a non-conductive adhesive material that physically secures the conductive lead to the bond pad, or alternately, an electrically conductive adhesive material that both physically and/or electrically couples the conductive lead to the bond pad. In an alternate embodiment, a **microelectronics** package includes a **microelectronics** device, an **interposer**, a plurality of conductive leads and a plurality of bond pads, and the reinforcement portion is disposed about a plurality of lead bonds. In this embodiment, the reinforcement portion may include a non-conductive adhesive material, or an anisotropically conductive material.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 6 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:356790 HCAPLUS
DN 134:347119
TI **Chip**-on-**chip** structure semiconductor device package
IN Den, Keiichi
PA Rohm Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 2001135783	A2	20010518	JP 1999-314083	19991104

AB The invention relates to a **chip**-on-**chip** structure semiconductor device package, wherein the metal films of the **chips** are interconnected to the contacts on the **heat sink** through **bonding wires** of the lead frame.

L34 ANSWER 7 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:295002 HCAPLUS
DN 134:304203
TI Design and fabrication of a stack package for a semiconductor memory device
IN Park, Sang Wook; Cho, Soon Jin
PA Hyundai Electronics Industries Co., Ltd., S. Korea
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6222259	B1	20010424	US 1999-393869	19990910
	KR 2000019697	A	20000415	KR 1998-37931	19980915
PRAI	KR 1998-37931	A	19980915		

AB Disclosed are a stack package and a method of manufg. the same. The stack package of the present invention comprises a ceramic capsule. A pair of protruding portions are formed at both upper sides of the ceramic capsule. A 1st semiconductor **chip** is attached on the upper face of the ceramic capsule and a 2nd semiconductor **chip** is attached on a lower face of the ceramic capsule. The 1st and 2nd semiconductor **chips** are disposed such that their bonding pads are disposed upwardly, more particularly the 2nd semiconductor **chip** has a size that its bonding pad may be exposed from both sides of the ceramic capsule. It is preferable to attach a **heat sink** at the lower face of the 2nd semiconductor **chip**. The 1st and 2nd semiconductor **chips** are elec. connected with a metal wire. A midway portion of the metal wire is laid on the protruding portion of the ceramic capsule. The entire resultant is encapsulated with a molding compd. while exposing the portion of metal wire laid on the protruding portion and the **heat sink**. A **conductive bump** is formed on the exposed portion of the metal wire, and a solder ball is mounted on the **conductive bump**.

RE.CNT 21 THERE ARE 21 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 8 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:279603 HCAPLUS
TI **Integrated circuit** package for flip **chip** and method of forming same
IN Panchou, Karen A.; Newton, Charles M.
PA Harris Corporation, USA
SO U.S., 6 pp., Division of Ser. No. US 1998-59080, filed on 13 Apr 1998
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6218214	B1	20010417	US 1999-422011	19991021

PRAI US 1998-59080 A3 19980413
AB An **integrated circuit** package includes a ceramic substrate having a cut out configured to receive a flip **chip**. The cut out includes vias formed as through holes. A flip **chip** is received within the cut out of the ceramic substrate and has **conductive bumps** formed thereon corresponding to the electrical input/output contacts of the flip **chip**. The **conductive bumps** are received within the through holes of the ceramic substrate. A second **integrated circuit chip** is mounted on the flip **chip** in back-to-back relationship. A controlled impedance line is secured to the **conductive bumps** and acts as a coax. In another aspect of the present invention, a **heat sink** can be mounted on the back of the flip **chip**, and the second **integrated circuit chip** mounted on the **heat sink**

RE.CNT 25 THERE ARE 25 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 9 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:221911 HCAPLUS
DN 134:246115
TI Method of making an organic **chip** carrier package
IN Bhatt, Anilkumar C.; Miller, Thomas R.; Moring, Allen F.; Walsh, James P.
PA International Business Machines Coporation, USA
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6207354	B1	20010327	US 1999-288052	19990407

AB A method of making a circuitized substrate wherein a **chip** -accommodating cavity is formed along with a plurality of **conductive** elements (e.g., **pads**, lines, etc.) which form part of the substrate's circuitry. Metalization is provided over the elements and, significantly, on the internal surfaces of the formed cavity to thereby enhance the elec. properties of the finished product, e.g., by assuring a solid, continuous path between upper and lower surfaces of the product.
RE.CNT 25 THERE ARE 25 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 10 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:73595 HCAPLUS
DN 134:140394
TI Fabrication of **wire bond** pads with single anchoring structures
IN Lin, Shi-Tron; Chan, Chin-Jong
PA Winbond Electronics Corp., Taiwan
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6181016	B1	20010130	US 1999-327877	19990608

	TW 441026	B	20010616	TW 2000-89107310 20000418
PRAI	US 1999-327876	A	19990608	
	US 1999-327877	A	19990608	

AB A bond pad structure is introduced for use in **wire bonding** applications during the packaging of semiconductor devices with reduced bond pad lift-off problem. It includes: (a) a laminated structure contg. a metal bond pad layer, a dielec. layer, and an underlying layer formed on a **wafer** surface; and (b) a single anchoring structure formed in the dielec. layer connecting the metal bond pad layer and the underlying layer. The single anchoring structure contains a plurality of line segments that are interconnected so as to form the single anchoring structure. Unlike prior art anchoring structures, which always contain a plurality of anchors buried inside the dielec., the bond pad structure contains only a single anchoring structure, which can have the geometry of an open or closed **ring** with whiskers, a coil, an open or closed square-waved **ring**, a tree structure, a grid-line structure, a meandering structure, a serpentine structure, a spiral structure, or a labyrinth. Also, an array of dendritic sub-structures can be provided extending from an outer edge of the anchoring structure to further improve stability.

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 11 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:819423 HCAPLUS
DN 133:358182
TI Rf shielded packaging for **integrated circuits**
IN Glenn, Thomas P.
PA Amkor Technology, Inc., USA
SO U.S., 22 pp., Cont.-in-part of U. S. 5,981,314.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6150193	A	20001121	US 1998-83524	19980522
	US 5981314	A	19991109	US 1996-741797	19961031
PRAI	US 1996-741797	A2	19961031		

AB A shielded package for an **IC chip** having bond pads thereon includes an insulating substrate having metalizations formed on a surface of the substrate. The **IC chip** is mounted to the substrate surface and the **IC chip bonding pads** are elec. coupled to corresponding substrate metalizations. An insulating encapsulant layer encapsulates the **IC chip** and the substrate surface. A conductive shield layer comprising a cured flowable elec. conductive material is formed above the encapsulant layer. The encapsulant layer elec. isolates the shield layer from the **IC chip** and the various elec. conductors (e.g. **bonding pads**, **bond wires**, **contacts** and metalizations). The shield layer, being an elec. conductive material, forms a floating ground plane which shields the **IC chip** and the remainder of the package. Thus, the shield layer prevents external radiation from interfering with the operation of the package and also prevents the package from emitting radiation which could interfere with other electronic components and devices.

RE.CNT 45 THERE ARE 45 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 12 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:779068 HCAPLUS
TI **Chip** c4 assembly improvement using magnetic force and adhesive
IN Downes, Francis J., Jr.; Japp, Robert M.; Pierson, Mark V.
PA International Business Machines Corporation, USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6142361	A	20001107	US 1999-458483	19991209

AB A method, and assocd. structure, for adhesively coupling a **chip** to an org. **chip** carrier. The **chip** is attached to a top surface of the org. **chip** carrier by interfacing a solder bump between a C4 solder structure on the **chip** and a pad on a top surface of the **chip** carrier. The melting temp. of the solder bump is less than the melting temp. of the C4 solder structure. A block of ferrous material is placed on a top surface of the **chip** . A temporary or permanent **stiffener** of ferrous material is placed on the top surface of the **chip** carrier. A permanent magnet is coupled to a bottom surface of the **chip** carrier. Alternatively, an electromagnetic could be utilized instead of the electromagnet. Due to the permanent magnet or the electromagnet, a magnetic force on the **stiffener** is directed toward the magnet and substantially flattens the first surface of the **chip** carrier. Similarly, a magnetic force on the block is directed toward the magnet such that the electronic component and the **chip** carrier are held in alignment. The solder bump is reflowed at a temp. between the melting temp. of the solder bump and the melting temp. of the C4 solder structure. The reflowing reconfigures the solder bump. The magnetic force on the block frictionally clamps the reflowed solder between the C4 solder structure and the pad. The **chip** and carrier are cooled, resulting in the C4 solder structure being adhesively and **conductively** coupled to the **pad**.
RE.CNT 31 THERE ARE 31 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 13 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:738861 HCAPLUS
DN 133:289978
TI **Microelectronic** connector with planar elastomer sockets
IN Fjelstad, Joseph
PA Tessera, Inc., USA
SO U.S., 24 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6133072	A	20001017	US 1997-987570	19971211
PRAI US 1996-33148	P	19961213		

AB A component for mounting semiconductor **chips** or other **microelectronic** units includes a compliant, sheet-like body with arrays of sheet-like **conductive pads** on upper and lower surfaces of the body. Flexible leads extending through the body interconnect **conductive pads** on the upper and lower

surfaces. The leads are desirably formed from wire, such as Au wire, that is bonded to the **conductive pads** using a **conductive** epoxy or a eutectic bonding alloy. The component is made using sacrificial base sheets having conductive terminal portions to which the leads are initially bonded. The compliant body is formed by injecting a flowable material between the base sheets, curing the material and removing the base sheets by etching. The flowable material surrounds the leads such that the leads are supported by the cured compliant layer. The component may be used as an **interposer** or as a test socket.

RE.CNT 52 THERE ARE 52 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 14 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:618779 HCAPLUS
DN 133:316016
TI Three-dimensional microanalysis of the wire-**pad contact** region of **integrated circuits**
AU Wu, H.; Takanashi, K.; Ono, N.; Cheng, Zh. H.; Sakamoto, T.; Sakou, T.; Owari, M.; Nihei, Y.
CS Institute of Industrial Science, The University of Tokyo, Tokyo, 106-8558, Japan
SO Surf. Interface Anal. (2000), 29(8), 508-513
CODEN: SIANDQ; ISSN: 0142-2421
PB John Wiley & Sons Ltd.
DT Journal
LA English
AB We have developed a three-dimensional microanalyzer by combination of a gallium focused ion beam (Ga-FIB), a secondary electron detector and a time-of-flight (ToF) mass spectrometer. The Ga-FIB can create successive flat cross-sections parallel to the interface. We performed ToF-SIMS mapping by switching the d.c. mode of the Ga-FIB in the cross-sectioning to pulse mode after turning the cross-section through 90. Combination of these ToF maps on each cross-section yields detailed three-dimensional information from the interface region. The Au **wire bonding** interface after heat treatment was analyzed. Anal. of the three-dimensional elemental distribution in the contact region of the Au wire and Al pad was realized. An Au-Al alloy was found in the deep section of the contact interface, Al was distributed in the outer part as a **ring** and the center part was enclosed by Au. The deduced structure of the contact region of the Au wire and Al pad was discussed.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 15 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:606773 HCAPLUS
DN 133:186517
TI Method of fabricating an **integrated-circuit** substrate for packages
IN Bhatt, Anilkumar Chinuprasad; Miller, Thomas Richard; Moring, Allen Frederick; Walsh, James Paul
PA International Business Machines Corporation, USA
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6110650	A	20000829	US 1998-42898	19980317

US 6225028 B1 20010501 US 2000-482548 20000113
PRAI US 1998-42898 A3 19980317
AB A method of making a circuitized substrate is claimed wherein a **chip**-accommodating cavity is formed along with a plurality of **conductive** elements (e.g., **pads**, lines, etc.) which form part of the substrate's circuitry. Metalization is facilitated using a photoimageable member that allows for initial removal (peeling) of its sacrificial layer, followed by eventual removal of the photoimaging layer which also forms part of this member. Exposure of the photoimaging layer may occur either through the protective sacrificial layer or subsequent removal thereof.
RE.CNT 21 THERE ARE 21 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 16 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:562579 HCAPLUS
TI Method for packaging **integrated circuits** with elastomer **chip** carriers
IN Son, Dae Woo; Lee, Youn Soo; Kim, Byung Man
PA Samsung Electronics, Co., Ltd., S. Korea
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6103554	A	20000815	US 1998-219015	19981223

PRAI KR 1998-290 A 19980108
AB A semiconductor **chip** packaging method includes the provision of individual elastomer **chip** carriers cut from an elastomer sheet having a uniform thickness and smooth, parallel surfaces. The elastomer sheet is mounted on an adhesive tape held by a fixing member, such as a support **ring**, and is then divided into individual carriers. The carrier is attached to a circuit **interposer**, and a semiconductor **chip** is attached to the carrier. Circuit leads of the **interposer** are bonded to connection pads on the **chip**. The beam lead bonding area is then encapsulated, and **conductive bumps** are formed on the underside of the package to serve as input/output terminals for the packaged device. Using this method, an number of devices can be packaged simultaneously on a flexible sheet and then separated into individual devices by cutting the sheet between the devices.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 17 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:483826 HCAPLUS
TI Assembly for dissipating heat from a stacked semiconductor package
IN Lee, Won Sang
PA Lg Electronics, Inc., S. Korea
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6091142	A	20000718	US 1997-991239	19971216

PRAI KR 1996-66223 A 19961216
AB A stacked semiconductor package and a method for assembling the same are disclosed, the stacked semiconductor package including a semiconductor **chip** having a plurality of **wire bonding pads** thereon; leads formed in a direction to electrically connect with the **wire bonding pads**; a **heat sink** connected to the predetermined **wire bonding pad** to **radiate** out **heat** of the semiconductor **chip**; and an epoxy supporting and protecting the semiconductor **chip**, the leads, and the **heat sink**.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 18 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:89157 HCAPLUS
TI Method for coupling substrates and structure
IN Grupen-Shemansky, Melissa E.; Lin, Jong-Kai; Tessier, Theodore G.
PA Motorola, Inc., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6022761	A	20000208	US 1996-654466	19960528

AB A method for connecting substrates includes using an adhesive **interposer** structure (11) to bond a semiconductor device (26) to a substrate (18). The adhesive **interposer** structure (11) includes a non-conductive adhesive laminant (12) and **conductive** adhesive **bumps** (13). The **conductive** adhesive **bumps** (13) provide a **conductive** path between **conductive bumps** (27) on the semiconductor device (26) and **conductive** metal **pads** (21) located on the substrate (18). In an alternative embodiment, a conductive adhesive material (34) is screen or stencil printed into vias (39) located on a printed circuit board (38) to form **conductive** adhesive **bumps** (33). A non-conductive adhesive (52) is then screen or stencil printed onto the printed circuit board (38) adjacent the **conductive** adhesive **bumps** (33). A semiconductor **die** is then connected to the structure.
RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 19 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:571983 HCAPLUS
TI Method of forming a **chip** scale package, and a tool used in forming the **chip** scale package
IN Razon, Eli; Von, Seggern Walter
PA Kulicke & Soffa Investments, USA
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5950070	A	19990907	US 1997-857708	19970515
	US 6136681	A	20001024	US 1999-322528	19990528
PRAI	US 1997-857708	A3	19970515		

AB A method of assembling a plurality of semiconductor **chips** is provided. A portion of a semiconductor **wafer** containing the plurality of **chips** is provided. Each of the plurality of **chips** has a contact pattern area including a pattern of contacts on a surface of the **chip**. A respective section of a dielectric **interposer** is assembled to each respective one of the plurality of **chips** individually, without detaching the plurality of **chips** from the portion of the semiconductor **wafer**. Each section of **interposer** has a plurality of **bonding pads** near an outer periphery of the section, so that each **bonding pad** lies near the contact pattern area of the corresponding one of the plurality of **chips**. Each **bonding pad** is **wire bonded** to a respective one of the contacts on the front surface of the corresponding one of the plurality of **chips**. The bonding step includes (1) bonding one end of each wire to a respective **bonding pad** of the **interposer** using micro-resistant welding or ultrasonic bonding, and (2) bonding the other end of each wire to a respective contact of the **chip** using ultrasonic bonding If a defective bond is detected, a wire may be removed and replaced by **wire bonding**. An encapsulant is applied to encapsulate the wires on each of the plurality of **chips**. The encapsulated **chips** are cut from the semiconductor **wafer**. **Wires** may be **bonded** at the corners of the **chip**, and need not be perpendicular to the sides of the **chip**.

L34 ANSWER 20 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:550386 HCAPLUS
DN 119:150386
TI **Bonding pad** for semiconductor device
IN Nakada, Takaaki
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05063021	A2	19930312	JP 1991-246819	19910830

AB A **bonding pad** for a semiconductor device, which is attached to a semiconductor **chip** and elec. connected with an external electrode through a **bonding wire**, consists of a central electrode and elec. isolated coaxial **ring** electrodes. The **bonding pad** can maintain a min. parasitic capacitance.

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SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Feb W1
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  File   6:NTIS  1964-2002/Feb W4
         (c) 2002 NTIS, Intl Cpyrght All Rights Res
*File   6: See HELP CODES6 for a short list of the Subject Heading Codes
(SC=, SH=) used in NTIS.
  File   8:Ei Compendex(R)  1970-2002/Feb W1
         (c) 2002 Engineering Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Feb W2
         (c) 2002 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2002/Feb
         (c) 2002 ProQuest Info&Learning
  File  77:Conference Papers Index  1973-2002/Jan
         (c) 2002 Cambridge Sci Abs
  File  94:JICST-EPlus  1985-2002/Dec W5
         (c)2002 Japan Science and Tech Corp(JST)
*File  94: There is no data missing. UDs have been adjusted to reflect
 the current months data. See Help News94 for details.
  File  99:Wilson Appl. Sci & Tech Abs  1983-2001/Dec
         (c) 2002 The HW Wilson Co.
  File 108:AEROSPACE DATABASE  1962-2001/DEC
         (c) 2002 AIAA
*File 108: For update information please see Help News108.
  File 144:Pascal  1973-2002/Feb W1
         (c) 2002 INIST/CNRS
  File 238:Abs. in New Tech & Eng.  1981-2002/Jan
         (c) 2002 Reed-Elsevier (UK) Ltd.
  File 305:Analytical Abstracts  1980-2002/Feb W1
         (c) 2002 Royal Soc Chemistry
*File 305: Frequency of updates and Alerts changing to weekly.
See HELP NEWS 305.
  File 315:ChemEng & Biotec Abs  1970-2002/Dec
         (c) 2002 DECHEMA
  File  14:Mechanical Engineering Abs  1973-2002/Jan
         (c) 2002 Cambridge Sci Abs
  File  65:Inside Conferences  1993-2002/Feb W1
         (c) 2002 BLDSC all rts. reserv.
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Set	Items	Description
S1	10723	BALL()GRID? ? OR BALLGRID? OR BGA OR BGAS OR PBGAS OR PBGA OR CGA OR CGAS
S2	2692	(SOLDER OR SOLDERING OR SOLDERED OR BRAZ?)(2N)(BALL OR BALLS OR PADS OR PAD OR SPHERE? ?)
S3	230923	(HEAT? OR WARM? OR HOT? ? OR THERMOL? OR THERMAL? OR PREHEAT? OR MELT? OR FUSE? ? OR FUSING? ? OR FUSION?)(3N)(SPREAD? - OR CIRCULATE? OR DISPERS? OR DISTRIBUT? OR RADIAT? OR SCATTER? OR COVER? OR OVERLAY?)
S4	674102	HEAT?()SINK? OR RING? ? OR INTERPOSER? OR STIFFENER?
S5	3809	((RAIS? OR INCREAS? OR ELEVAT?)(2N)(TEMP? ? OR TEMPERATUR?-))(3N)(SPREAD? OR CIRCULATE? OR DISPERS? OR DISTRIBUT? OR RADIAT? OR SCATTER? OR COVER? OR OVERLAY?)
S6	43883	(CIRCUIT)(2N)(BOARD? ?) OR (SYSTEM? ?()BOARD? ?) OR MOTHERBOARD? OR MOTHER()BOARD?
S7	200640	SOLDER OR SOLDERING OR SOLDERED OR BRAZ?
S8	1587139	IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT? ?)) OR (MICRO)(W)(CIRCUIT? ? OR CHIP? ? OR ELECTRONIC?) OR CHIP? ? OR MICROCIRCUIT? ? OR DIE? ? OR LOGIC(W) CIRCUIT? ? OR WAFER? ? OR MICROELECTRONIC?
S9	71164	CC=B2570 Semiconductor integrated circuits
S10	3542	(CONTACT? OR BONDING)(2N)(PAD OR PADS OR BUMP OR BUMPS)
S11	10614	(WIRE OR WIRES OR LINE OR LINES)(2N)(BOND?)
S12	269	(CONDUCTIV?)(3N)(BUMP? OR PAD OR PADS)
S13	6667258	ENCLOS??? OR HOUS??? OR CASE? ? OR CONTAIN? OR ENCASE? OR ENCAPSUL? OR PACKAG?
S14	6725	S1 AND S13
S15	472	S14 AND (S3:S5)
S16	98	S15 AND S2
S17	34	S16 AND S6
S18	20	RD (unique items)
S19	4568	S14 AND (S8 OR S9)
S20	392	S19 AND (S3:S5)
S21	9	S20 AND S10
S22	44	S20 AND S11
S23	33	RD (unique items)
S24	29	S23 NOT (S18 OR S21)
S25	7	S21 NOT S18

? T S18/3,AB/1-5
>>>No matching display code(s) found in file(s): 65

18/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6736775 INSPEC Abstract Number: B2000-12-0170J-007
Title: Flip chip wafer level **packaging** of a flexible chip scale **package** (CSP)
Author(s): Hotchkiss, G.; Amador, G.; Edwards, D.; Hundt, P.; Stark, L.; Stierman, R.; Heinen, G.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3906 p.555-62
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3906L.555:FCWL;1-J
Material Identity Number: C574-2000-070
Conference Title: 1999 International Symposium on Microelectronics
Conference Sponsor: IMAPS
Conference Date: 26-28 Oct. 1999 Conference Location: Chicago, IL, USA
Language: English
Abstract: The advent of chip scale **packages** (CSP) within the semiconductor community has led to the development of wafer scale assembly (WSA) or wafer level **packaging** (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip chip, **ball grid** array **packages** . The die inputs and outputs of the TI CSP are connected through solder bumps to a polyimide film **interposer**. **Solder balls** on the other side of the **interposer** complete the electrical connection to a customer's printed **circuit board** . A wafer-sized array of **interposers** designed to match the pattern of dies on a wafer is aligned and reflowed to a bumped wafer. The TI WLP process is completed by singulating the CSP's from the wafer using standard wafer saw equipment. Attachment of the **interposer** to the die as well as applying the die and board level solder bumps are carried out in wave form using a new bumping technology called Tacky Dots/sup TM/. Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polymide film for transferring and attaching **solder spheres** to semiconductor substrates. A populated film **containing** one **solder sphere** per tacky dot is positioned over the wafer or **interposer** and lowered until the spheres contact the pads. A reflow process transfers the spheres from the film to the wafer or **interposer** and the film is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed for forming the TI CSP. The strategic use of finite element modeling for optimizing the design of the **package** is outlined. The paper concludes by summarizing the current **package** level reliability results.
Subfile: B

18/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6724574 INSPEC Abstract Number: B2000-11-0170J-082, C2000-11-7410D-132
Title: An investigation of thermal enhancement on flip chip plastic **BGA packages** using CFD tool
Author(s): Lee, T.-Y.
Author Affiliation: Interconnect Syst. Labs., Motorola Inc., Tempe, AZ, USA
Journal: IEEE Transactions on Components and Packaging Technologies vol.23, no.3 p.481-9
Publisher: IEEE,
Publication Date: Sept. 2000 Country of Publication: USA
CODEN: ITCPFB ISSN: 1521-3331
SICI: 1521-3331(200009)23:3L.481:ITEF;1-1
Material Identity Number: H324-2000-004
U.S. Copyright Clearance Center Code: 1521-3331/2000/$10.00
Language: English
Abstract: This paper demonstrates the advantage of applying Predictive Engineering in the thermal assessment of a 279 inputs/outputs (I/Os), six-layer, depopulated array flip chip **PBGA package**. Thermal simulation was conducted using a computational fluid dynamics (CFD) tool to analyze the heat transfer and fluid flow in a free convection environment. This study first describes the modeling techniques on a multilayer substrate, thermal vias, solder bumps, and printed **circuit board** (PCB). For a flip chip **package** without any thermal enhancement, more than 90% of the total power was conducted from the front surface of the die through the **solder ball** interconnects to the substrate, then to the board. To enhance the thermal performance of the **package**, the heat transfer area from the backside of the die needs to increase dramatically. Several thermal enhancing techniques were examined. These methods included a copper **heat spreader** with various thicknesses and with thermal pads, metallic lid, overmolded with and without a **heat** spreader, and with **heat sink**. An aluminum lid and a **heat sink** gave the best improvement; followed by a **heat spreader** with **thermal** pads. Both methods reduced thermal resistance by an average of 50%. Detailed analyses on heat flow projections are discussed.
Subfile: B C

18/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6715227 INSPEC Abstract Number: B2000-11-0170J-041
Title: Effects of lead bonding process on reliability of chip scale **package**
Author(s): Lee, Y.J.; Eyre, M.W.
Author Affiliation: Electron. Packaging Mater. Dev., Dow Corning Corp., Midland, MI, USA
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070) p.1392-7
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xxxv+1756 pp.
ISBN: 0 7803 5908 9 Material Identity Number: XX-2000-01366
U.S. Copyright Clearance Center Code: 0 7803 5908 9/2000/$10.00
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, and Manuf. Technol. Soc. of

IEEE; Electronic Ind. Alliance
Conference Date: 21-24 May 2000 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: An integrated circuit (IC) **package** has become smaller and its profile becomes lower as new chip scale **packaging** (CSP) designs have been introduced. A new design of **packages** demands new materials and optimization of manufacturing processes to enhance reliability of the **package**. A compliant layer in Tessera's mu -**BGA**(R) **package** is a crucial component to increase **solder ball** reliability in the board level assembly. The compliant layer can reduce damage to the **solder balls**, which is induced by mismatch of the coefficient of thermal expansion (CTE) between Si die and the printed **circuit board** (PCB). Silicone elastomer is one of the best candidate for the compliant layer due to its low modulus and low moisture absorption. While the colder ball reliability in the mu -**BGA** **package** is significantly improved due to its unique design and optimal materials set, fatigue damage can be imposed on beam leads inside of the **package** during thermal cycling. To reduce the damage in the **package** , an optimal lead (or beam lead) bonding process becomes critical for flex circuit **interposer** type of CSP designs including mu -**BGA** . Three dimensional (3D) Finite Element Analysis (FEA) of the lead bonding and subsequent thermal cycling, is conducted to show effects of designs of the lead (dimensions and shapes) as well as the lead bonding process parameters. Several different loci of a bond tool motion are numerically simulated to determine optimal lead bonding parameters based on the calculated damage accumulated in the deformed shape of leads during the lead bonding process followed by the thermal cyclings.
Subfile: B

18/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6693406 INSPEC Abstract Number: B2000-10-0170J-037
Title: Impact properties of **PBGA** assemblies reflowed in nitrogen ambient and compressed air
Author(s): Wu, Y.P.; Chan, Y.C.
Author Affiliation: Dept. of Electron. Eng., City Univ. of Hong Kong, China
Journal: IEEE Transactions on Advanced Packaging vol.23, no.3 p. 421-5
Publisher: IEEE,
Publication Date: Aug. 2000 Country of Publication: USA
CODEN: ITAPFZ ISSN: 1521-3323
SICI: 1521-3323(200008)23:3L.421:IPPA;1-O
Material Identity Number: H273-2000-003
U.S. Copyright Clearance Center Code: 1521-3323/2000/$10.00
Language: English
Abstract: In this paper, the solder joint brittleness of plastic **ball grid** array (**PBGA**) assemblies has been studied by means of impact testing. The results show that the maximum impact force and the impact energy for **PBGA** assemblies reflowed in nitrogen ambient is higher than for those reflowed in compressed air. Reduction of the oxygen content from 1000 ppm to 50 ppm, reduces the initiation energy of impact. The impact fractured surfaces occur between the printed **circuit board** (PCB) **pads** and **solder** joints, i.e., in the brittle

intermetallics region. The pores and impurities are mainly distributed within a **ring** at perimeter of the interface, with greater density at the edges than at the center. Reflow in a nitrogen ambient reduces the defect density, with reduction in oxygen content further reducing the density. Impact cracks begin from the defects of the Cu/solder interface, and propagate along the intermetallics.
Subfile: B
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18/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC
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6493755 INSPEC Abstract Number: B2000-03-0170J-170
Title: Effect of **heat-spreader** sizes on the **thermal** performance of large cavity-down plastic **ball grid** array **packages**
Author(s): Lau, J.; Chen, T.; Lee, S.-W.R.
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Journal: Transactions of the ASME. Journal of Electronic Packaging vol.121, no.4 p.242-8
Publisher: ASME,
Publication Date: Dec. 1999 Country of Publication: USA
CODEN: JEPAE4 ISSN: 1043-7398
SICI: 1043-7398(199912)121:4L.242:EHSS;1-5
Material Identity Number: N602-2000-001
Language: English
Abstract: The effect of **heat-spreader** size on the temperature **distribution**, **thermal** resistance, and cooling power of a set of cost-effective cavity-down plastic **ball grid** array (**PBGA**) **packages** assembled on a FR-4 epoxy glass printed **circuit board** (PCB) is presented. The sizes of these **packages** are 35*35 mm and 40*40 mm, with 4 and 5 rows of **solder balls**.
Subfile: B
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? T S18/3,AB/6-9
>>>No matching display code(s) found in file(s): 65

18/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC
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6319767 INSPEC Abstract Number: B1999-09-0170J-103, C1999-09-7410D-083
Title: Optimizing cost and thermal performance: rapid prototyping of a high pin count cavity-up enhanced plastic **ball grid** array (EPBGA) **package**
Author(s): Zahn, B.A.
Author Affiliation: Package Characterization Lab., ChipPAC Inc., Chandler, AZ, USA
Conference Title: Fifteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.99CH36306) p.133-41
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA xvi+299 pp.
ISBN: 0 7803 5264 5 Material Identity Number: XX-1999-01041
U.S. Copyright Clearance Center Code: 0 7803 5264 5/99/$10.00
Conference Title: Fifteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium. SEMI-THERM. Proceedings 1999
Conference Sponsor: IEEE Components, Packaging, & Manuf. Technol. Soc

Conference Date: 9-11 March 1999 Conference Location: San Diego, CA, USA
Language: English
Abstract: A three-dimensional finite element model of a 420 lead (5 row perimeter) cavity-up enhanced plastic **ball grid** array (EPBGA) **package** was developed using the ANSYS/sup TM/ finite element simulation code. The developed model was utilized to perform a sensitivity analysis in order to quantify the effects of varying **package** and system **motherboard** designs. Design variables included: (1) chip size; (2) **package** substrate metallized plane layers; (3) **motherboard** metallized plane layers; (4) inner **solder ball** matrix and vias; (5) **package** aluminum **heat spreader** thickness; and (6) chip power dissipation. Predicted **package** junction-to-ambient thermal resistance (theta /sub JA/) values were used in conjunction with a central composite design of experiments to develop a response surface equation which quickly predicts EPBGA **package** thermal performance as a function of the six design variables. The methodology described allows for rapid analysis of design options in the "dynamic" environment of prototyping, and the implementation of optimized cost effective **package** designs to meet required standards under multiple customer environments.
Subfile: B C

18/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

6271398 INSPEC Abstract Number: B1999-07-0170J-191
Title: Effect of **heat-spreader** sizes on the **thermal** performance of large cavity-down plastic **ball grid** array **packages**-NuBGA
Author(s): Lau, J.; Chen, T.
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Journal: Microelectronics International vol.16, no.2 p.24-33
Publisher: MCB University Press,
Publication Date: April 1999 Country of Publication: UK
CODEN: MIINF2 ISSN: 1356-5362
SICI: 1356-5362(199904)16:2L.24:EHSS;1-E
Material Identity Number: D084-1999-002
Language: English
Abstract: The effect of **heat-spreader** size on the temperature **distribution**, **thermal** resistance, and cooling power of a set of cost-effective cavity-down plastic **ball grid** array (**PBGA**) **packages**, NuBGA, assembled on an FR-4 epoxy glass printed **circuit board** (PCB) is presented, from the results of a finite element analysis study. The sizes of these **packages** are 35*35 mm and 40*40 mm and with four and five rows of **solder balls**.
Subfile: B

18/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

6266193 INSPEC Abstract Number: B1999-07-0170J-083
Title: Thermal fatigue analysis for solder bump in **BGA**

packages
Author(s): Iwasaki, K.; Ikemizu, M.; Ando, T.; Mukai, M.; Kawakami, T.
Author Affiliation: Semicond. Adv. Packaging Eng. Dept., Toshiba Corp., Kawasaki, Japan
Conference Title: Advances in Electronic Packaging 1997. Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference. INTERpack '97 Part vol.2 p.1775-81 vol.2
Editor(s): Suhir, E.; Shiratori, M.; Lee, Y.C.; Subbarayan, G.
Publisher: ASME, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 2 vol. xxi+2223 pp.
ISBN: 0 7918 1559 5 Material Identity Number: XX-1999-01000
Conference Title: Proceedings of InterPACK '97
Conference Sponsor: ASME
Conference Date: 15-19 June 1997 Conference Location: Kohala Coast, HI, USA
Language: English
Abstract: This paper discusses the design optimization of **ball grid** array (**BGA**) **packages** with the help of FEM analysis, placing a special emphasis on **solder ball** reliability and **package** warpage after board assembly. The **solder ball** interconnection between **BGA package** and printed **circuit board** (PCB) is susceptible to shear stress during thermal storage due to the mismatch in coefficient of thermal expansion (CTE) between them. Compared to other **BGAs**, Tape **Ball Grid** Array (TBGA) has lower thermal resistance and lower impedance as well as the greater capability of accommodating fairly high counts of I/Os. Therefore, an extensive study was given in regard to the optimization of TBGA structure. In TBGA, a metal plate called **stiffener** is installed to improve the ability of keeping the **package** flat. An adhesive material to attach the TAB tape and the **stiffener** plays the role of stress buffer which is caused from the thermal mismatch between the **package** and PCB. Two crucial issues are associated with the design optimization of the **package** . One is the improvement of solder joint reliability and the other is the prevention of **package** warpage. In this study, elastic-creep analyses of solder bumps and elastic analyses of **package** coplanarity were performed. The largest creep strain among all solder bumps was calculated using both a global **package** model and a local model. Then thermal fatigue life was estimated from the Coffin-Manson's equation which was obtained from a low cycle fatigue test. A number of analyses were carried out varying thickness and the CTE of the **stiffener**. Thickness of the **stiffener** tuned out to be the most influential factor on **package** warpage. Also we found, compared to the effect from thickness, the CTE of the **stiffener** has much greater effect on solder bump stress. In conclusion, significant progress was achieved in TBGA design optimization and we believe the methodology in this study can also be applied to the design of any other **BGA package**.
Subfile: B

18/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

6250800 INSPEC Abstract Number: B1999-06-0170J-154
Title: Optimization of high pin count cavity-up enhanced plastic **ball grid** array (EPBGA) **packages** for robust design

Author(s): Mertol, A.
Author Affiliation: LSI Logic Corp., Fremont, CA, USA
Conference Title: Advances in Electronic Packaging 1997. Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference. INTERpack '97 Part vol.1 p.1079-88 vol.1
Editor(s): Suhir, E.; Shiratori, M.; Lee, Y.C.; Subbarayan, G.
Publisher: ASME, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 2 vol. xxi+2223 pp.
ISBN: 0 7918 1559 5 Material Identity Number: XX-1997-01724
Conference Title: Proceedings of InterPACK '97
Conference Sponsor: ASME
Conference Date: 15-19 June 1997 Conference Location: Kohala Coast, HI, USA
Language: English
Abstract: Three dimensional nonlinear finite element models of epoxy **encapsulated** enhanced plastic **ball grid** array (EPBGA) **packages** with and without an aluminum lid have been developed using ANSYS/sup TM/ finite element simulation code. The model has been used to optimize the **packages** for robust design and to determine design rules to keep **package** warpage within acceptable limits, An L/sub 18/ Taguchi matrix has been developed to investigate the effect of die attach and **encapsulant** properties along with the substrate, **encapsulant**, die attach, and internal copper plane thicknesses on the reliability of the **package** during temperature cycling. For **package** failures, simulations performed represent temperature cycling from 165 degrees C to -65 degrees C. This condition is approximated by cooling the **package** mounted on a multilayer printed **circuit board** (PCB) from 165 degrees C to -65 degrees C. For coplanarity analysis, simulations have been performed without the PCB and the lowest temperature of the cycle is changed to 20 degrees C. Predicted results indicate that for an optimum design, that is low stress in the **package** and low **package** warpage, **encapsulant** as well as die attach material should have low Young's modulus and low coefficient of thermal expansion. Furthermore, it is found that the substrate and the die attach epoxy thicknesses should be increased beyond the current design. In addition to the optimization analysis, plastic strain distribution on each **solder ball** has been determined to predict the location of the possible first **solder ball** failure. The results indicate that higher strain levels are attained in **solder balls** underneath the die region. Even if there were any **solder ball** failures in that region it would not affect the functionality of the **package** since the **solder balls** in that region are used only for thermal enhancement of the **package**. For the **package** with an aluminum lid, although significantly higher solder bail strain is observed at the dam **ring** location, the magnitudes are still much lower than the ones observed underneath the die region.
Subfile: B

? T S18/3,AB/10-15
>>>No matching display code(s) found in file(s): 65

18/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

6128186 INSPEC Abstract Number: B1999-02-0170J-088
Title: S-TBGA: A cost effective alternative to enhanced **PBGAs**
Author(s): Karnezos, M.

Author Affiliation: Signetics KP, San Jose, CA, USA
Conference Title: Proceedings of the Technical Program. NEPCON West '98. Conference Part vol.3 p.1412-23 vol.3
Publisher: Reed Exhibition, Norwalk, CT, USA
Publication Date: 1998 Country of Publication: USA 3 vol. 1546 pp.
Material Identity Number: XX-1998-02004
Conference Title: Proceedings of NEPCON West 98
Conference Date: 1-5 March 1998 Conference Location: Anaheim, CA, USA
Language: English
Abstract: S-TBGA is a cavity down **BGA** that provides superior power dissipation and equivalent electrical performance compared to a four-layer enhanced **PBGA** at competitive cost. It uses a thin flex interconnect substrate with one metal layer and an integral **heat spreader** with ground plane. The die is attached to the **heat spreader**, the ground pads are wire bonded to the cavity ground **ring**, and the ground **solder balls** are reflowed directly on the ground plane. This low inductance plane is used for all ground connections and carries all ground currents. All signal and power connections are via the flex substrate. The low **package** profile at 1.35 mm thick and the **heat spreader** which **covers** the whole **package** surface provide an effective EMI shield and reduce noise. The combination of single-metal tape with ground plane offers the high electrical performance of a two-metal tape at a fraction of the cost. Direct die attachment to a Cu **heat spreader** provides the lowest **thermal** resistance, carrying about 50% of the heat to ambient. The remaining heat is conducted through the 0.15 mm thin substrate and the **solder balls** to the **motherboard**. The 60 mu m high density routing of the substrate allows routing of up to seven rows of **solder balls** in a single metal layer with finest usable bond finger pitch of 100 mu m, short wires <1.2 mm, large maximum die size and no minimum die size specification. The combination of single-metal tape and stamped **heat spreader** /ground plane assembly allow for a high performance **package** at low cost for high volume applications. Special design features, **package** structure and assembly process are discussed and performance data are given.
Subfile: B

18/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

6010654 INSPEC Abstract Number: B9810-0170J-038
Title: Tape **ball grid** array with ground plane
Author(s): Karnezos, M.
Author Affiliation: Signetics High Technol. Inc., San Jose, CA, USA
Conference Title: Area Array Packaging Technologies. Workshop on Flip Chip, CSP and Ball Grid Arrays p.111-24
Publisher: Fraunhofer Inst. Reliability & Microintegration, Berlin, Germany
Publication Date: 1997 Country of Publication: Germany 304 pp.
Material Identity Number: XX98-00095
Conference Title: Proceedings of Area Array Packaging Technologies Workshop on Flip Chip and Ball Grid Arrays
Conference Date: 17-19 Nov. 1997 Conference Location: Berlin, Germany
Language: English
Abstract: The Signetics-tape **ball grid** array (S-TBGA) is a cavity down **BGA** using a copper/polyimide flex interconnect substrate

and a copper **heat spreader** assembly which serves as the ground plane and also as the tape carrier/**stiffener**. The flex substrate, with a pitch of 60 mu m, is capable of routing up to seven rows of **solder balls** at 1.27 mm pitch, allowing maximum ball count for a fixed body size. The minimum bond pitch on the **package** is limited to 110 mu m only by the wire bonding process capabilities, yet reduces wire lengths down to 1.5 mm to produce very low inductance signal connections. Direct reflow of **solder balls** on the ground plane and direct wire bonds from the die to the ground **ring** provide a very low inductance plane for all the ground connections. The combination of a single-metal tape with ground plane offers the high electrical performance of the two-metal tape, but at a fraction of the cost. The low **package** profile at 1.35 mm thickness and a **heat spreader** which **covers** the whole **package** surface provide a very effective EMI shield and reduce noise. The direct attachment of the die against the copper **heat spreader** provides for the lowest possible thermal resistance, carrying about 50% of the heat to the ambient. The remaining heat is conducted through the 0.15 mm thin tape and the numerous **solder balls** to the **motherboard**. The combination of the single-metal tape and the stamped **heat spreader**/ground plane assembly allow for a high performance **package** at low enough cost for high volume applications.

Subfile: B

18/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

5704138 INSPEC Abstract Number: B9711-0170J-028

Title: Investigation of **heat sink** attach methodologies and the effects on **package** structural integrity and interconnect reliability of the 119-lead plastic **ball grid** array

Author(s): Eyman, L.M.; Kromann, G.B.
Author Affiliation: Motorola Inc., Austin, TX, USA

Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.1068-75
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 1294 pp.
ISBN: 0 7803 3857 X Material Identity Number: XX97-01595
U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00
Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA
Language: English

Abstract: An experimental study was performed to investigate various **heat sinks** and attach methods commercially available for the high-performance 119-lead plastic **ball grid** array (**PBGA**) **package** . Attach methods investigated in this study include a pressure-sensitive adhesive, mechanical clips, and thermally conductive adhesives. This work will show the effects of **heat sink** attach methods on the **package** structural integrity and **solder ball** interconnect reliability. This work is necessary to better provide total solutions for customers who will need to dissipate high levels of power from this **package**. The **heat sinks** were attached to the 119-lead **PBGA packages** which were mounted on

multi-layer printed-**circuit boards**. These assemblies were then subjected to accelerated-life testing (ALT) using air-to-air thermal cycling between 0 degrees C and 100 degrees C to determine the effect of attaching **heat sinks** to the **packages** on the electrical reliability of the solder joint connection. Besides interconnect reliability, ALT was used to determine the effect of thermal cycling on the reliability of the **heat sink** attach mechanism. The **heat sink** attach mechanisms were tested by three different methods. The first was to simply observe the **heat sinks** to see if they fall off during thermal cycling. Mechanical shock tests then were performed using a **package** drop tester. Samples that underwent 1000, 2000, and 11400 thermal cycles, as well as no thermal cycling, were subjected to this test. Finally, shear strength tests using a constant strain-rate mechanical testing machine were performed on the **packages** with **heat sinks** attached using adhesives. Several modes of failure appeared in the experiments. These failures included extremely low interconnect life in thermal cycling, **heat sink** detachment during drop tests and during thermal cycling, and low adhesion strength in shear tests. While some attachment methods were obviously not suitable, others provided robust solutions to the **heat sink** attachment problem.

Subfile: B

18/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

5678314 INSPEC Abstract Number: B9710-0170J-031

Title: Reliability results for a wire bondable tape **ball grid** array **package**

Author(s): Schueller, R.D.

Author Affiliation: 3M Electron. Prod. Div., Austin, TX, USA

Conference Title: SMTA National Symposium `Emerging Packaging Technologies' Proceedings of The Technical Program p.71-85

Publisher: Surface Mount Techol. Assoc, Edina, MN, USA

Publication Date: 1996 Country of Publication: USA 138 pp.

Material Identity Number: XX96-03693

Conference Title: Proceedings of Technology in the Park Symposium

Conference Date: 18-21 Nov. 1996 Conference Location: Research Triangle Park, NC, USA

Language: English

Abstract: This paper reviews a new wire bondable tape **ball grid** array **package** which exhibits a cost/performance advantage in the industry. This novel **package** architecture utilizes the fine line capability of flexible circuitry to provide the high performance and reliability required by the increasingly advanced ICs of today and tomorrow. This TBGA is designed to provide excellent heat dissipation through use of a **heat spreader** to which the die is directly adhered. Heat is therefore efficiently dissipated into surrounding air and into the **motherboard**. With the capability for less than 50 mu m lines and spaces, the wire bond fingers can be moved in very close to the die, thus minimizing wire bond length and allowing for the possibility of die shrinkage. The resulting decrease in inductance enables **packaging** of high speed devices. This product can be provided at a competitive price, partially due to 3M's efficient process for simultaneous chemical etching of holes in the polyimide substrate to define **solder ball pads**. This paper includes an overview of this **package** as well as detailed results of **package** coplanarity and board level

reliability testing. Extrapolations are performed to estimate life in actual use conditions. These results show ample reliability for most applications.
Subfile: B

18/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

5436516 INSPEC Abstract Number: B9701-0170J-082
Title: Thermal performance comparison of high pin count cavity-up enhanced plastic **ball grid** array (EPBGA) **packages**
Author(s): Mertol, A.
Author Affiliation: LSI Logic Corp., Fremont, CA, USA
Conference Title: Inter-Society Conference on Thermal Phenomena in Electronic Systems, I-THERM V (Cat. No.96CH35940) p.140-50
Publisher: IEEE, New York, NY,, USA
Publication Date: 1996 Country of Publication: USA xxi+407 pp.
ISBN: 0 7803 3325 X Material Identity Number: XX96-02358
U.S. Copyright Clearance Center Code: 0 7803 3325 X/96/$5.00
Conference Title: InterSociety Conference on Thermal Phenomena in Electronic Systems, I-THERM V
Conference Sponsor: K-16 Committee on Heat Transfer in Electron. Equipment, Heat Transfer Div., ASME; Electron. Packag. Div., ASME; Components, Packag. & Manuf. Technol. Soc. IEEE; NIST, U.S. Dept. Commerce
Conference Date: 29 May-1 June 1996 Conference Location: Orlando, FL, USA
Language: English
Abstract: Three dimensional finite element models of cavity-up enhanced plastic **ball grid** array (EPBGA) **packages** have been developed using ANSYS/sup TM/ finite element simulation code. The models have been used for thermal characterization of different designs of high pin count EPBGA **packages** under different air flow conditions with and without an external **heat sink** . In addition to the design evaluations, the simulations have been repeated to quantify the effect of populated and unpopulated boards on the thermal performance of each EPBGA **package** with and without a **heat sink**. For the unpopulated board **case**, a single **package** has been modeled on a 10 cm*10 cm*0.16 cm (4"s 4"*0.062") multilayer printed **circuit board** (PCB). For the populated board, the size has been reduced to the size of the **package** footprint, and no heat transfer is permitted along the board periphery. Further parametric studies have been performed to predict the thermal performance of EPBGA **packages** as a function of **solder ball** counts in the inner **solder ball** matrix (underneath the cavity). In conjunction, the optimum number of **solder balls** in the inner matrix has been determined for better heat dissipation through the **package** to the board via the thermal balls. In addition to the **solder ball** counts, the importance of the **package** internal vias connected to the **solder balls** in the inner matrix is quantified.
Subfile: B

18/3,AB/15 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05828916
E.I. No: EIP01236533587
Title: Wafer level **packaging** of a tape flip-chip chip scale **packages**
Author: Hotchkiss, G.; Amador, G.; Edwards, D.; Hundt, P.; Stark, L.; Stierman, R.; Heinen, G.
Corporate Source: Texas Instruments Incorporated MS 940, Dallas, TX 75265, United States
Source: Microelectronics and Reliability v 41 n 5 May 2001 2001. p 705-713
Publication Year: 2001
CODEN: MCRLAS ISSN: 0026-2714
Language: English
Abstract: The advent of chip scale **packages** (CSPs) within the semiconductor community has led to the development of wafer scale assembly (WSA) or wafer level **packaging** (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip-chip, **ball grid** array **packages**. The die inputs and outputs of the TI CSP are connected through solder bumps to a polyimide film **interposer**. **Solder balls** on the other side of the **interposer** complete the electrical connection to a customer's printed **circuit board**. A wafer-sized array of **interposers** designed to match the pattern of dies on a wafer is aligned and reflowed to a bumped wafer. The TI WLP process is completed by singulating the CSPs from the wafer using standard wafer saw equipment. Attachment of the **interposer** to the die as well as applying the die and board level solder bumps are carried out in wafer form using a new bumping technology called Tacky Dots trademark . Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polyimide film for transferring and attaching **solder spheres** to semiconductor substrates. A populated film **containing** one **solder sphere** per Tacky Dot is positioned over the wafer or **interposer** and lowered until the spheres contact the pads. A reflow process transfers the spheres from the film to the wafer or **interposer** and the film is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed for forming the TI CSP. The strategic use of finite element modeling for optimizing the design of the **package** is outlined. The paper concludes by summarizing the current **package** level reliability results. copy 2001 Elsevier Science Ltd. 13 Refs.
? T S18/3,AB/16-20
>>>No matching display code(s) found in file(s): 65

18/3,AB/16 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04471981
E.I. No: EIP96083285140
Title: Flex tape **ball grid** array
Author: Karnezos, Marcos; Goetz, Martin; Dong, Fred; Ciaschi, Andrew; Chidambaram, N.
Corporate Source: ASAT Inc, Palo Alto, CA, USA
Conference Title: Proceedings of the 1996 IEEE 46th Electronic Components & Technology Conference, ECTC
Conference Location: Orlando, FL, USA Conference Date: 19960528-19960531
E.I. Conference No.: 45119

Source: Proceedings - Electronic Components and Technology Conference 1996. p 1271-1277
Publication Year: 1996
CODEN: PECCA7 ISSN: 0569-5503
Language: English
Abstract: Flex Tape **Ball Grid** Array (FTBGA) is a family of cavity down **BGAs**. The die, the flex tape and the **solder balls** are attached to the bottom side of a metallic heatspreader that acts as the **stiffener** and carrier of the **package**. The die is wire bonded to the tape traces and then **encapsulated**. The thermal and electrical performance and reliability are clearly superior to the alternative Plastic **Ball Grid** Arrays (**PBGAs**), the conventional plastic and thermally enhanced QFPs. The **packages** are constructed from materials that are well established in the industry. They are assembled using the same equipment, tools and processes as for the assembly of **PBGAs**. (Author abstract) 9 Refs.

18/3,AB/17 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04471973
E.I. No: EIP96083285132
Title: Reliability evaluations on a new tape **ball grid** array (TBGA)
Author: Gainey, Trevor; Stover, Mike; Auray, Michel
Corporate Source: LSI Logic Europe plc
Conference Title: Proceedings of the 1996 IEEE 46th Electronic Components & Technology Conference, ECTC
Conference Location: Orlando, FL, USA Conference Date: 19960528-19960531
E.I. Conference No.: 45119
Source: Proceedings - Electronic Components and Technology Conference 1996. p 1217-1221
Publication Year: 1996
CODEN: PECCA7 ISSN: 0569-5503
Language: English
Abstract: Results of a co-operative study of a new type of Tape **Ball Grid** Array (TBGA) are reported. Results obtained by a component manufacturer (LSI Logic) in reliability assessment of this new **package** type are reported together with results obtained during board mounting trials and subsequent reliability stress testing at board level by a system assembly **house** (Bull Electronics Europe). The various test techniques used by the component manufacturer during component qualification will be described and discussed in terms of the potential failure mechanisms detected by each of the stress tests. Likewise the various electrical, thermal and mechanical tests applied to the mounted **package** are also discussed in relationship to the end use environment. Results are presented of **package** level tests together with those of **packages** mounted to boards both with and without an external heatsink. The study concludes that with careful **package** design and construction together with good board assembly and heatsink attachment methods applied to the **package**, a highly reliable **package** and board assembly system can be achieved. (Author abstract) 4 Refs.

18/3,AB/18 (Item 4 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

04471971
E.I. No: EIP96083285130
Title: Reliability characterization of the SLICC **package**
Author: Lall, Pradeep; Gold, Glenn; Miles, Barry; Banerji, Kingshuk; Thompson, Pat; Koehler, Corey; Adhihetty, Indira
Corporate Source: Motorola, Inc, Plantation, FL, USA
Conference Title: Proceedings of the 1996 IEEE 46th Electronic Components & Technology Conference, ECTC
Conference Location: Orlando, FL, USA Conference Date: 19960528-19960531
E.I. Conference No.: 45119
Source: Proceedings - Electronic Components and Technology Conference 1996. p 1202-1210
Publication Year: 1996
CODEN: PECCA7 ISSN: 0569-5503
Language: English
Abstract: SLICC (Slightly Larger than IC Carrier) is a chip-scale **ball grid** array (**BGA**) **package** currently under development at Motorola. The SLICC **package** consists of a solder-bumped integrated circuit (IC) which is flip-chip bonded to an **interposer** substrate - approximately 8 mils thick - and then underfilled with an **encapsulant**. Chip I/Os are routed to **package** I/Os through plated through holes (PTHs) in the **interposer** substrate. **Package** I/Os are composed of solder bumps (approx. 22.2 mils in diameter on a 32-mil pitch) attached to the bottom side of the **interposer** substrate. The most apparent benefit of the SLICC **package** is its utilization of the area efficiency associated with direct chirp attach (DCA) technology, coupled with the assembly, test, and repair simplicity afforded by **BGA**-type **packaging**. Architectural details of the SLICC **package** can be found in references left bracket Banerji, 1994; Banerji and Lall, 1995 right bracket (Author abstract) 8 Refs.

18/3,AB/19 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14087813 PASCAL No.: 99-0280975
Effect of **heat-spreader** sizes on the **thermal** performance of large cavity-down plastic **ball grid** array **packages** : NuCSP
LAU J; CHEN T
Express Packaging Systems, Inc., Palo Alto, California, United States
Journal: Microelectronics international, 1999, 16 (2) 24-33
Language: English
The effect of **heat-spreader** sizes on the temperature **distribution**, **thermal** resistance, and cooling power of a set of cost-effective cavity-down plastic **ball grid** array (**PBGA**) **packages** assembled on an FR-4 epoxy glass printed **circuit board** (PCB) is presented. The sizes of these **packages** are 35 x 35mm and 40 x 40mm and with four and five rows of **solder balls**.

18/3,AB/20 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

13417634 PASCAL No.: 98-0110896
Optimization of high pin count cavity-up enhanced plastic **ball grid** array (EPDGA) **packages** for robust design
MERTOL A
LSI Logic Corporation, Fremont, CA 94539, United States
Journal: IEEE transactions on components, packaging, and manufacturing technology. Part B, Advanced packaging, 1997, 20 (4) 376-388
Language: English
Three-dimensional (3-D) nonlinear finite element models of epoxy **encapsulated** enhanced plastic **ball grid** array (EPBGA) **packages** with and without an aluminum lid have been developed using ANSYS finite element simulation code (1). The model has been used to optimize the **packages** for robust design and to determine design rules to keep **package** warpage within acceptable limits. An L SUB 1 SUB 8 Taguchi matrix has been developed to investigate the effect of die attach and **encapsulant** properties along with the substrate, **encapsulant**, die attach, and internal copper plane thicknesses on the reliability of the **package** during temperature cycling. For **package** failures, simulations performed represent temperature cycling from 165 Degree C to -65 Degree C. This condition is approximated by cooling the **package** mounted on a multilayer printed **circuit board** (PCB) from 165 Degree C to -65 Degree C. For coplanarity analysis, simulations have been performed without the PCB and the lowest temperature of the cycle is changed to 20 Degree C. Predicted results indicate that for an optimum design, that is low stress in the **package** and low **package** warpage, **encapsulant** as well as die attach material should have low Young's modulus and low coefficient of thermal expansion. Furthermore, it is found that the substrate and the die attach epoxy thicknesses should be increased beyond the current design. In addition to the optimization analysis, plastic strain distribution on each **solder ball** has been determined to predict the location of the possible first **solder ball** failure. The results indicate that higher strain levels are attained in **solder balls** underneath the die region. Even if there were any **solder ball** failures in that region it would not affect the functionality of the **package** since the **solder balls** in that region are used only for thermal enhancement of the **package**. For the **package** with an aluminum lid, although significantly higher **solder ball** strain is observed at the dam **ring** location, the magnitudes are still much lower than the ones observed underneath the die region.

? T S25/3,AB/1-7
>>>No matching display code(s) found in file(s): 65

25/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7074086 INSPEC Abstract Number: B2001-12-0170J-009
Title: Advanced **wafer** level CSP **packaging** using new liquid bismaleimide polymers
Author(s): Wakabayashi, T.; Kuwabara, O.; Lan Wu; Sagami, Y.; Santos, B.; Burkhart, A.
Author Affiliation: IEP Technol. Inc., Tokyo, Japan
Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.119-27
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2001 Country of Publication: USA 520 pp.
Material Identity Number: XX-2000-03037
Conference Title: Proceedings of 6th Annual Pan Pacific Microelectronics Symposium
Conference Sponsor: IMAPS; ITRI; Japan Inst. Electron. Packaging, Semicond. Equipment & Mater. Int.; et al
Conference Date: 13-16 Feb. 2001 Conference Location: Kauai, HI, USA
Language: English
Abstract: General interconnection technologies between **chips** and substrates which are currently very popular for semiconductors include COB, **BGA**, flip **chip**, etc., which use wirebonding and also flip **chip bump bonding** through the help of **interposers** made of laminate, ceramics and also tapes. This conventional technology has prevailed for the past few years. On the other hand, the new **wafer** level CSP **package** approach described here using novel liquid bismaleimide polymers exhibits many technical advantages over previous **packaging** technologies. It does not require the use of **interposers** , as it is directly mounted on the mother board, and also helps to meet the continued demand for **package** miniaturization.
Subfile: B

25/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7055042 INSPEC Abstract Number: B2001-11-0170J-097
Title: Underfill characterization for flip **chip BGA** featuring use of a rigid substrate
Author(s): Sakamoto, K.
Author Affiliation: Texas Instrum. Japan Ltd., Oita, Japan
Conference Title: SMTA International Proceedings of the Technical Program p.193-8
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2000 Country of Publication: USA 952 pp.
Material Identity Number: XX-2000-01486
Conference Title: Proceedings of SMTA International
Conference Date: 24-28 Sept. 2000 Conference Location: Rosemont, IL, USA
Language: English
Abstract: Flip **chip** interconnection has recently attracted attention since it is able to overcome the restrictions faced by

conventional wire bonding interconnections. High-pin count and high-performance devices can benefit greatly by reducing the **die** size by means of area array arrangement of **bonding pads** and by supplying power from the central part of the **die** to avoid a voltage drop. The first generation of flip **chip BGA** used a ceramic substrate as **interposer**, but a coefficient of thermal expansion (CTE) mismatch between the ceramic substrate and PWB might cause board level reliability problems. Using a socket is a solution which can avoid this stress, but it is also very expensive. In order to eliminate the socket, a rigid substrate is essential. Furthermore, it has the potential capability to improve the electrical performance since a copper pattern is utilized. However, the stress between **die** and substrate may result in serious reliability problems such as cracked **die** and delamination. An underfill material is thus used between **die** and substrate. This study aims to evaluate the underfill manufacturability and to investigate the material properties in order to improve productivity and minimize stress.
Subfile: B

25/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6946449 INSPEC Abstract Number: B2001-07-0170J-080
Title: **Wafer** level **packaging** of a tape flip-**chip** **chip** scale **packages**
Author(s): Hotchkiss, G.; Amador, G.; Edwards, D.; Hundt, P.; Stark, L.; Stierman, R.; Heinen, G.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Journal: Microelectronics Reliability vol.41, no.5 p.705-13
Publisher: Elsevier,
Publication Date: May 2001 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(200105)41:5L.705:WLPT;1-O
Material Identity Number: G489-2001-005
U.S. Copyright Clearance Center Code: 0026-2714/2001/$20.00
Language: English
Abstract: The advent of **chip** scale **packages** (CSPs) has led to the development of **wafer** scale assembly (WSA) or **wafer** level **packaging** (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip-**chip** **ball** **grid** array **packages**. The **die** inputs and outputs of the TI CSP are connected through solder bumps to a polyimide film **interposer**. Solder balls on the other side of the **interposer** complete the electrical connection to the PCB. A **wafer**-sized array of **interposers** designed to match the **wafer** **die** pattern is aligned and reflowed to a bumped **wafer** . The TI WLP process is completed by singulating the CSPs from the **wafer** using standard **wafer** saw equipment. Attachment of the **interposer** to the **die** and application of **die** and board level solder bumps are carried out in **wafer** form using a new bumping technology called Tacky Dots/sup TM/. Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polyimide film for transferring and attaching solder spheres to semiconductor substrates. A populated film **containing** one solder sphere per Tacky Dot is positioned over the **wafer** or **interposer** and lowered until the spheres **contact** the **pads**. A reflow process transfers the spheres from film to **wafer** or **interposer**

and the film is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed to form the TI CSP. Strategic use of finite element modeling to optimize the **package** design is outlined. The paper concludes by summarizing **package** level reliability results.
Subfile: B

25/3,AB/4 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09825502 Genuine Article#: 454VA Number of References: 13
Title: **Wafer** level **packaging** of a tape flip-**chip** **chip** scale **packages** (ABSTRACT AVAILABLE)
Author(s): Hotchkiss G (REPRINT) ; Amador G; Edwards D; Hundt P; Stark L; Stierman R; Heinen G
Corporate Source: Texas Instruments Inc,POB 655012,MS 940/Dallas//TX/75265 (REPRINT); Texas Instruments Inc,Dallas//TX/75265
Journal: MICROELECTRONICS RELIABILITY, 2001, V41, N5 (MAY), P705-713
ISSN: 0026-2714 Publication date: 20010500
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD OX5 1GB, ENGLAND
Language: English Document Type: ARTICLE
Abstract: The advent of **chip** scale **packages** (CSPs) within the semiconductor community has led to the development of **wafer** scale assembly (WSA) or **wafer** level **packaging** (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip-**chip**, **ball grid** array **packages**. The **die** inputs and outputs of the TI CSP are connected through solder bumps to a polyimide film **interposer**. Solder balls on the other side of the **interposer** complete the electrical connection to a customer's printed circuit board. A **wafer**-sized array of **interposers** designed to match the pattern of **dies** on a **wafer** is aligned and reflowed to a bumped **wafer**. The TI WLP process is completed by singulating the CSPs from the **wafer** using standard **wafer** saw equipment.

Attachment of the **interposer** to the **die** as well as applying the **die** and board level solder bumps are carried out in **wafer** form using a new bumping technology called Tacky Dots (TM). Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polyimide film for transferring and attaching solder spheres to semiconductor substrates. A populated film **containing** one solder sphere per Tacky Dot is positioned over the **wafer** or **interposer** and lowered until the spheres **contact** the **pads**. A reflow process transfers the spheres from the film to the **wafer** or **interposer** and the film is removed once the spheres have frozen.

This paper illustrates the process steps and custom equipment developed for forming the TI CSP. The strategic use of finite element modeling for optimizing the design of the **package** is outlined. The paper concludes by summarizing the current **package** level reliability results. (C) 2001 Elsevier Science Ltd. All rights reserved.

25/3,AB/5 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04167860 JICST ACCESSION NUMBER: 99A0565809 FILE SEGMENT: JICST-E
Packaging technology guidebook 1999. Summary of **packaging** technologies, such as CSP, buildup substrate, and soldering. 4. **BGA**/CSP. "VS-contact" probe technique for **wafer**-level CSP.
KIYOFUJI HIDEHIRO (1)
(1) Nihonmaikuronikusu
Denshi Zairyo(Electronic Parts and Materials), 1999, 5gatsugo bessatsu, PAGE.96-102, FIG.12
JOURNAL NUMBER: F0040AAH ISSN NO: 0387-0774
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: A conventional solder bump inspection causes solder bump crushing and reflow processing after the inspection has been indispensable. This paper introduces "VS-contact" probe card developed by Japan Micronics that can achieve contacts with little impact on solder **bump** shapes. The **contact** of "VS-contact" is **ring**-shaped, and wires are fanned out by using anisotropy electroconductive rubber and multilayer substrate. The structure of the contact, contact track left by the experimentally produced probe card, and frequency characteristics are shown.

25/3,AB/6 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15043946 PASCAL No.: 01-0201455
Wafer level **packaging** of a tape flip-**chip** **chip** scale **packages**
HOTCHKISS G; AMADOR G; EDWARDS D; HUNDT P; STARK L; STIERMAN R; HEINEN G
Texas Instruments Incorporated MS 940, Dallas, TX 75265, United States
Journal: Microelectronics and Reliability, 2001, 41 (5) 705-713
Language: English
The advent of **chip** scale **packages** (CSPs) within the semiconductor community has led to the development of **wafer** scale assembly (WSA) or **wafer** level **packaging** (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip-**chip**, **ball** **grid** array **packages**. The **die** inputs and outputs of the TI CSP are connected through solder bumps to a polyimide film **interposer**. Solder balls on the other side of the **interposer** complete the electrical connection to a customer's printed circuit board. A **wafer**-sized array of **interposers** designed to match the pattern of **dies** on a **wafer** is aligned and reflowed to a bumped **wafer** . The TI WLP process is completed by singulating the CSPs from the **wafer** using standard **wafer** saw equipment. Attachment of the **interposer** to the **die** as well as applying the **die** and board level solder bumps are carried out in **wafer** form using a new bumping technology called Tacky Dots Degree trademark<pilcrow>. Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polyimide film for transferring and attaching solder spheres

to semiconductor substrates. A populated film **containing** one solder sphere per Tacky Dot is positioned over the **wafer** or **interposer** and lowered until the spheres **contact** the **pads**. A reflow process transfers the spheres from the film to the **wafer** or **interposer** and the film is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed for forming the TI CSP. The strategic use of finite element modeling for optimizing the design of the **package** is outlined. The paper concludes by summarizing the current **package** level reliability results. (c) 2001 Elsevier Science Ltd.

25/3,AB/7 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

14460948 PASCAL No.: 00-0120698
Flip **Chip** **Wafer** Level **Packaging** of a flexible **Chip** Scale **package** (CSP)
IMAPS : international symposium on **microelectronics** : Chicago IL, 26-28 October 1999
HOTCHKISS G; AMADOR G; EDWARDS D; HUNDT P; STARK L; STIERMAN R; HEINEN G
Texas Instruments Incorporated, P.O. Box 655012, MS 940, Dallas, TX 75265, United States
International Society for Optical Engineering, Bellingham WA, United States.; International Microelectronics and Packaging Society, United States.
International symposium on microelectronics (Chicago IL USA) 1999-10-26
Journal: SPIE proceedings series, 1999, 3906 555-562
Language: English
The advent of **Chip** Scale **Packages** (CSP) within the semiconductor community has led to the development of **Wafer** Scale Assembly (WSA) or **Wafer** Level **Packaging** (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip **chip**, **ball** **grid** array **packages**. The **die** inputs and outputs of the TI CSP are connected through solder bumps to a polyimide film **interposer**. Solder balls on the other side of the **interposer** complete the electrical connection to a customer's printed circuit board. A **wafer**-sized array of **interposers** designed to match the pattern of **dies** on a **wafer** is aligned and reflowed to a bumped **wafer** . The TI WLP process is completed by singulating the CSP's from the **wafer** using standard **wafer** saw equipment. Attachment of the **interposer** to the **die** as well as applying the **die** and board level solder bumps are carried out in **wafer** form using a new bumping technology called Tacky Dots SUP < SUP T SUP M >. Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polyimide film for transferring and attaching solder spheres to semiconductor substrates. A populated film **containing** one solder sphere per tacky dot is positioned over the **wafer** or **interposer** and lowered until the spheres **contact** the **pads**. A reflow process transfers the spheres from the film to the **wafer** or **interposer** and the film is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed for forming the TI CSP. The strategic use of finite element modeling for optimizing the design of the **package** is outlined. The paper concludes by summarizing the current **package** level reliability results.

? T S24/3,AB/1-6
>>>No matching display code(s) found in file(s): 65

24/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7074087 INSPEC Abstract Number: B2001-12-0170J-010
Title: **IC package** solutions for high performance memory
Author(s): Solberg, V.
Author Affiliation: Tessera Inc., San Jose, CA, USA
Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.128-35
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2001 Country of Publication: USA 520 pp.
Material Identity Number: XX-2000-03037
Conference Title: Proceedings of 6th Annual Pan Pacific Microelectronics Symposium
Conference Sponsor: IMAPS; ITRI; Japan Inst. Electron. Packaging, Semicond. Equipment & Mater. Int.; et al
Conference Date: 13-16 Feb. 2001 Conference Location: Kauai, HI, USA
Language: English
Abstract: The market demand for **chip**-scale and **chip**-size **BGA packaging** for **ICs** is expanding rapidly. Proving to be fundamentally important to both current and future electronics, the array contact format is efficient for interconnection to the circuit board and the small component outline and lower profile (typical of these devices) is ideal for higher component density electronic applications. The higher processing speed of current electronics requires a very direct signal path and interconnection between controller, processor and memory. The newest generations of Rambus RDRAM memory technology, for example, have been developed to be compatible with a special new **chip** set from Intel, furnishing processing speeds exceeding 1 GHz, almost twice the speed of the PC processors. To meet the need for **packaging** of silicon **die** for these faster processing speeds, Tessera has developed a two-sided copper, flexible polyimide film-based **interposer** substrate employing laser ablated micro-vias. The **chip**-size **package** (unlike face-up **wire bonded** or direct **chip** attachment **package** structures), relies on the proven compliant mu **BGA**/sup (R)/ material system for both reliability and performance. The two metal layer **interposer** structure supplies a very direct **die**-to-ball contact interconnect and a robust ground plane within the finished **package**. The paper outlines the process steps and design attributes that enable the fabrication of one and two metal layer flex-based **interposers** and the **die packaging** process.
Subfile: B

24/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6777149 INSPEC Abstract Number: B2001-01-0170J-069
Title: Assessment of liquid **encapsulated** and transfer molded wirebonded cavity filled **packages**
Author(s): Ryan, L.; Lynch, B.; Babiarz, A.J.
Author Affiliation: Electron. Mater. Div., Dexter Corp., City of Industry, CA, USA

Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.275-80
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2000 Country of Publication: USA 423 pp.
Material Identity Number: XX-2000-01481
Conference Title: Proceedings of Fifth Annual Pan Pacific Microelectronics Symposium
Conference Sponsor: GPD
Conference Date: 25-27 Jan. 2000 Conference Location: Maui, HI, USA
Language: English
Abstract: Thermally enhanced **PBGAs** are typically cavity down and wirebonded. The majority of heat is extracted through the back of the **die** which is attached with a conductive adhesive to a metal **heat sink**. These **packages** are designed for heat dissipation on high power or high-speed **chips**. Typical I/O counts of these single or multi-tiered substrates exceed 300. Staggered **wire bond** pads with effective pitches down to 45 mu m are becoming more common. The **encapsulant** and **encapsulation** process must be optimized to eliminate voiding or "bridging" of the material over the wires. Nearly all of these **packages** use a fine filler liquid **encapsulant** at this time. The materials have been optimized to flow through very fine spaces at atmospheric pressure. Also, various liquid dispensing nozzles and dispense techniques have been developed to further increase production throughput. **Packages** of this type have been in low volume production for over five years. Liquid **encapsulants**, dispense processes and equipment have continued to improve as **package** volumes have increased. As progress is made to increase functionality and speed of devices, thermal problems become more pronounced and the use of these **packages** increases. High volume suppliers have gone from 1998 rates of about 300,000 devices per month to better than 1,000,000 per month in 1999. As semiconductor **packagers** increase production rates on these **packages** , the alternative of transfer molding these devices becomes more viable. This paper addresses the advantages and disadvantages of both processes as a function of both total **package** cost and **package** reliability.
Subfile: B

24/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6595807 INSPEC Abstract Number: B2000-06-6230B-007
Title: A new 16*16 ATM switching multichip module with high performance
Author(s): Youngmin Lee; Dong-Eun Chung; Sang-Pok Lee; Chul-Won Ju; Na, J.H.; Seong-Su Park; Min Kyu Song
Author Affiliation: Lab. for Micro-Electron., Electron. & Telecommun. Res. Inst., Taejon, South Korea
Journal: International Journal of Microcircuits and Electronic Packaging vol.22, no.4 p.440-5
Publisher: IMAPS-Int. Microelectron. & Packaging Soc,
Publication Date: 1999 Country of Publication: USA
CODEN: IMEPE5 ISSN: 1063-1674
SICI: 1063-1674(1999)22:4L.440:1SMM;1-O
Material Identity Number: P802-2000-002
Language: English
Abstract: Multichip module (MCM) **packaging** technology has been used for the ATM (asynchronous transfer mode) switching system since it provides

high throughput performance and miniaturization of the electronic system. The authors have developed a new MCM for a 16*16 ATM switching element, which handles a signal throughput of 2.4 Gpbs, routing 16 trunk lines of 155 Mbps. The new MCM which comprises three **chips** of 16*16 mm/sup 2/ in size individually mounted on a 48*48 mm/sup 2/ substrate was constructed with a high power 491 pin **PBGA**. As there are many **chip**-to-**chip** and substrate-to-**package** interconnect nets, including more than 1500 **wire bonds**, the researchers used an MCM-D substrate fabricated using a Cu/BCB multilayer process to minimize the total net lengths. One of the important things in this work is consideration of the thermal management issue. The heat dissipation from three **chips** exceeds 15.6 W total, so the 491 **PBGA** was specially designed in order for the generated heat to sink out effectively through a metal slug. In addition, more than 360 thermal vias under each **chip** attach area were formed in the MCM-D substrate. The MCM electrical test was sequentially performed in three steps including interconnect open/short of the substrate, BST (boundary scan test) and functional module performance. Adoption of the new 16*16 ATM switch MCM is expected to reduce the **package** footprint to less than 45% of that of the present switch system. Accordingly, the new ATM switch system could be miniaturized cost-effectively.
Subfile: B

24/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6519928 INSPEC Abstract Number: B2000-04-0170J-046
Title: Assembly and reliability of a new flex-based fine pitch **BGA**
Author(s): Hayden, T.F.; Clatanoff, W.J.; Del Rosario, E.; Opiniano, E.
Author Affiliation: Electron. Products Div., 3M Co., Austin, TX, USA
Conference Title: IPC Chip Scale and BGA National Symposium. Proceedings. Pursuit of the Perfect Package Part vol.1 p.177-83 vol.1
Publisher: IPC, Northbrook, IL, USA
Publication Date: 1998 Country of Publication: USA 2 vol. 183+96 pp.
Material Identity Number: XX-1999-01212
Conference Title: Proceedings of IPC Chip Scale/Ball Grid Array National Symposium
Conference Date: 6-7 May 1999 Conference Location: Santa Clara, CA, USA
Language: English
Abstract: This study demonstrates that a new small form factor, flex-based **BGA**/CSP **package** on 0.5 mm ball pitch (a) fits with the existing **IC package** assembly equipment infrastructure, and (b) survives board-level reliability for potential cellular phone applications. The **package** substrate consists of 3M flexible circuitry laminated to a metal **interposer-stiffener** . Assembly of the subject 7 mm, 64 I/O **packages** at Hana used traditional leadframe-like and **PBGA**-like **package** assembly processes of **die** attachment, gold ball **wire bonding**, overmolding, solder ball attachment and **package** singulation. The flexible circuit takes advantage of the high resolution capability of flex, enabling the routing of dense ball arrays and minimizing **package** size. The **stiffener** component of the electronic **package** increases the **package** CTE to closely match that of the PCB, as demonstrated by moire analysis, to reduce solder ball strain during board-level thermal cycling. Acceptable **package** assembly process performance data was obtained for the

subject 7 mm enhanced **BGA** including **die** shear, wire pull test, wire sweep, and solder ball shear data. All **package**-level reliability testing was successful, including air-to-air and liquid-to-liquid temperature cycling, high temperature storage, pressure cooker testing, and JEDEC Level 1 performance in moisture resistance testing. Board-level reliability testing is following the expected trend of increasing solder ball integrity (ball shear and board temperature cycling) with increasing **package** solder ball pad size.
Subfile: B

24/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6482587 INSPEC Abstract Number: B2000-03-2570-001
Title: Development of a 1000-pin fine-pitch **BGA** for high performance LSI
Author(s): Suwa, M.; Miwa, T.; Tsutsumi, Y.; Shirai, Y.
Author Affiliation: Device Dev. Center, Hitachi Ltd., Tokyo, Japan
Conference Title: 1999 Proceedings. 49th Electronic Components and Technology Conference (Cat. No.99CH36299) p.430-4
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA xxxii+1289 pp.
ISBN: 0 7803 5231 9 Material Identity Number: XX-1999-02031
U.S. Copyright Clearance Center Code: 0 7803 5231 9/99/$10.00
Conference Title: 1999 Proceedings. 49th Electronic Components and Technology Conference
Conference Date: 1-4 June 1999 Conference Location: San Diego, CA, USA
Language: English
Abstract: A 1000-pin fine-pitch **BGA** has been developed by using a 50- mu m ultra fine pitch **wire bonding** technique. This **package** can be mounted with a **chip** with dimensions ranging from 14 mm*14 mm to 16 mm*16 mm. This **package** also has signal lines that have an embedded microstrip line structure. Also it has a **package** size **heat spreader** , which means that the electrical characteristics are such that the **package** can be applied to an LSI operating at a frequency of about 800 MHz. The thermal characteristics are such that the **package** can be applied to 10 W devices without the need for a fin. Furthermore, this **BGA package** has been confirmed to be sufficiently reliable.
Subfile: B

24/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

6282607 INSPEC Abstract Number: B1999-08-0170J-016, C1999-08-7410D-024
Title: Parametric study of thermal performance of a plastic **ball grid** array, single **package** technology for automotive applications
Author(s): Ramakrishna, K.; Trent, J.R.
Author Affiliation: Adv. Interconnect Syst. Labs., Motorola Inc., Austin, TX, USA
Conference Title: CAE/CAD and Thermal Management Issues in Electronic Systems. 1997 ASME International Mechanical Engineering Congress and

Exposition p.13-21
Editor(s): Agonafer, D.; Amon, C.H.; Belady, C.; Kowalski, G.; Orgega, A.
Publisher: ASME, New York, NY, USA
Publication Date: 1997 Country of Publication: USA v+109 pp.
ISBN: 0 7918 1852 7 Material Identity Number: XX-1999-00994
Conference Title: CAE/CAD and Thermal Management Issues in Electronic Systems. ASME International Mechanical Engineering Congress and Exposition
Conference Sponsor: ASME
Conference Date: 16-21 Nov. 1997 Conference Location: Dallas, TX, USA
Language: English
Abstract: Thermal performance of a three **chip BGA** single **package** technology (SPT) has been evaluated under horizontal natural convection conditions for under-the-hood automotive applications by solving a conjugate heat transfer problem to determine the maximum junction temperatures as a function of ambient temperature and material parameters. The resulting conjugate heat transfer problem is solved using computational fluid dynamics (CFD) methods. The SPT provides **packaging** of all dice on a single **wire bonded** plastic **ball grid** array (**PBGA**) four layer BT substrate. All dice are **encapsulated** in a single mold compound block. The SPT is attached to a 1.52 mm thick, four-layer (with two solid internal copper planes) FR4 PWB. The multi-dimensional heat transfer effects in the vias and the C5 solder joints are taken into account through a separate sub-model approach and the effective conductivity is used in the CFD model. The actual stack-ups of the BT substrate and PWB are used in the CFD analysis. Radiative loss from the exposed surfaces of the **package** and the PWB to the ambient is included. Since the objective here is the assessment of stand-alone **package** level thermal performance of the SPT, it is assumed that no other components are dissipating power on the PWB. The transient conjugate problem is also solved for power up of the **package** initially at an ambient temperature of 125 degrees C for a power dissipation of 7 W. CFD simulations of the transient have been carried out for 7 s after the **die** is powered up.

? T S24/3,AB/7-29
>>>No matching display code(s) found in file(s): 65

24/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

6111921 INSPEC Abstract Number: B9901-0170J-167
Title: Development of fine pitch **ball grid** array
Author(s): Shibata, J.; Horita, M.; Izumi, N.; Shikano, T.; Okada, M.; Noguchi, Y.; Imamura, K.; Fukunaga, H.; Yasunaga, M.; Hirai, T.; Hashimoto, T.; Takemoto, Y.
Author Affiliation: Mitsubishi Electr. Corp., Hyogo, Japan
Conference Title: 2nd 1998 IEMT/IMC Symposium (IEEE Cat. No.98EX225) p.45-9
Publisher: Organizing Committee 1998 IEMT/IMC Symposium, Tokyo, Japan
Publication Date: 1998 Country of Publication: Japan xvii+391 pp.
ISBN: 0 7803 5090 1 Material Identity Number: XX98-02086
Conference Title: 2nd 1998 IEMT/IMC Symposium
Conference Sponsor: IEEE CPMT (Components, Packaging, & Manuf. Technol.) Soc.; SHM: Microelectron. Soc.-Japan (IMAPS-Japan)
Conference Date: 15-17 April 1998 Conference Location: Tokyo, Japan
Language: English
Abstract: A fine pitch **ball grid** array (FBGA) has been developed which is suitable mainly for logic devices such as micro control units (MCU) and application specific **integrated circuits** (ASIC) for consumer portable electronic instruments. The FBGA has a construction in which a **die** is attached to a glass-epoxy **interposer** with a single layer conductor. **Wire bonding** and transfer molding are applied in the same manner as lead frame type **packages**. The FBGA has a smaller body and higher performance than conventional **packages**. The **package** structure, assembly process, performance and reliability test results are introduced.
Subfile: B

24/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

6091405 INSPEC Abstract Number: B9901-0170J-029
Title: Performance and reliability of a cavity down tape **BGA package**
Author(s): Schueller, R.D.; Aeschliman, D.; Chiew, T.H.
Author Affiliation: 3M Electron. Products Div., Austin, TX, USA
Conference Title: Proceedings of the 1997 1st Electronic Packaging Technology Conference (Cat. No.97TH8307) p.151-62
Editor(s): Tay, A.A.O.; Beng, L.T.
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 319 pp.
ISBN: 0 7803 4157 0 Material Identity Number: XX98-02804
U.S. Copyright Clearance Center Code: 0 7803 4157 0/97/$10.00
Conference Title: Proceedings of the 1997 1st Electronic Packaging Technology Conference
Conference Sponsor: Inst. Mater. Res. & Eng.; Inst. Microelectron.; IEEE CPMT Soc
Conference Date: 8-10 Oct. 1997 Conference Location: Singapore
Language: English

Abstract: As the demand for greater I/O has increased, so has the interest in **ball grid** array **packaging** . It is well recognized in the **packaging** industry that as the pin counts increase above 208, **BGA packages** become more attractive due to their small form factor and ease of board attach. However, along with the general trend for higher I/O, an increasing percentage of **ICs** are also running at over 200 MHz and 4 W of power. These **IC** requirements surpass the capability of standard QFP and **PBGA packages**. To satisfy this demand, there has been a major push for high performance **BGA packages** which are considerably more cost effective than ceramic **package** alternatives. Tape **BGA packages** provide an excellent cost/performance solution in this market segment and are gaining a great deal of attention. With the fine line capability of flexible circuits (down to 25 mu m lines and spaces), the **wire bond** fingers can be moved very close to the **die**. This enables **die** shrinkage in pad limited **die** and reduces wire length, which is often the main source of **package** self inductance. Excellent thermal properties are achieved by directly attaching the **die** to a thermally conductive copper **stiffener** or **heat spreader**.
The copper CTE also matches closely with that of the board to maximize thermal cycle reliability. This product can be provided at a competitive price due to the minimization of materials and a simplified production process. The result is a low cost, high performance **package** with excellent reliability. This paper discusses the electrical and thermal performance of this **package** along with the reliability.
Subfile: B

24/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

6049268 INSPEC Abstract Number: B9811-0170J-056
Title: Manufacturing process for combination lead frame/TAB **BGA**
Author(s): Mita, M.; Murakami, G.; Kumakura, T.; Kashiwabara, F.
Author Affiliation: Densen Works, Hitachi Cable Ltd., Ibaraki, Japan
Journal: IEEE Transactions on Components, Packaging & Manufacturing Technology, Part C (Manufacturing) vol.21, no.3 p.204-10
Publisher: IEEE,
Publication Date: July 1998 Country of Publication: USA
CODEN: ITCMF2 ISSN: 1083-4400
SICI: 1083-4400(199807)21:3L.204:MPCL;1-U
Material Identity Number: D485-98004
U.S. Copyright Clearance Center Code: 1083-4400/98/$10.00
Language: English
Abstract: The combination lead frame/tape automated bonding **ball grid** array (TAB **BGA**) has been studied to improve the manufacturability of thin **ball grid** array (TBGA) large scale integrated (LSI) **packages** . Ordinary lead frames and the TAB tape carriers have been applied to make the assembly of TBGA easier. The base technologies, the materials of the lead frame, and the TAB tape were thoroughly applied to the **heat spreader** and the fine routing flexible substrate. The lead frames as the **heat spreader** and the tape (manufactured by the line of the TAB tape for **wire bonding** substrate) are combined with a high thermal resistive adhesive (Tg473K). As the solder balls are reflowed prior to **die** attach, current assembly **houses** will never need the ball mounter to produce the TBGA.

Subfile: B

24/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

6031412 INSPEC Abstract Number: B9811-0170J-011
Title: **Chip** scale or flip scale: the wrong question? [area array **packaging**]
Author(s): Gilleo, K.
Author Affiliation: Cookson Electron., Cranston, RI, USA
Journal: Circuits Assembly vol.9, no.2 p.30, 32-4
Publisher: Miller Freeman,
Publication Date: Feb. 1998 Country of Publication: USA
CODEN: CIATE5 ISSN: 1054-0407
SICI: 1054-0407(199802)9:2L.30:CSFS;1-L
Material Identity Number: O602-98007
U.S. Copyright Clearance Center Code: 1054-0407/98/$2.00+0.25
Language: English
Abstract: DCA-I (direct **chip** attach-on-**interposer**), micro-flip-**chip** **ball grid** array (**BGA**), or whatever title is given to the flip **chip**-on-**interposer** structure, is moving rapidly into the **chip** scale **packaging** (CSP) arena as an effective, low cost and friendly micro-**package**. The flip **chip** character of the **package** becomes transparent to the assembler, as it becomes a surface mount **package** that is soldered with standard equipment using a familiar process. The product is now becoming available from major companies such as Amkor and Motorola. A gradual shift in **BGA** manufacturing from **wire bonding** to flip **chips** is likely. Due to its extreme versatility, **wire bonding** will continue to be a mainstream process in the foreseeable future, but the ease in producing CSPs with flip-**chip** technology could very well make flip-**chip** CSP the dominant micro-**package** in the future.
Subfile: B

24/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

6016055 INSPEC Abstract Number: B9810-0170J-078
Title: Advanced **packaging** solution for high-performance system-on-**chip** applications: Flip-**chip** **BGA**
Author(s): Liao, J.-M.; Wang, W.
Author Affiliation: Fujitsu Microelectron. Inc., San Jose, CA, USA
Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.43-9
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 1998 Country of Publication: USA 508 pp.
Material Identity Number: XX98-00364
Conference Title: Proceedings of Pan Pacific Microelectronics Symposium
Conference Sponsor: Surface Mount Technol. Assoc.; Int. Microelectron. & Packaging Soc.; Semicond. Equipment & Mater. Int
Conference Date: 10-13 Feb. 1998 Conference Location: Kona, HI, USA
Language: English
Abstract: High performance system-on-**chip** devices generally have a

large I/O count, high power dissipation, and run at a high clock rate. To meet these requirements, an advanced **packaging** solution flip-**chip** **ball grid** array (FCBGA) was developed. As I/O count increases, the interconnection from **die** to the **package** migrates from the peripheral **wire** **bond** to flip **chip** bond that provides enhanced signal wireability and electrical performance. For high I/O count **packages**, **BGAs** provide the interconnection from the **package** to the board with excellent thermal and electrical performance at a moderate cost. **Package** thermal enhancement can be accomplished by attaching the **heat** **spreader** directly to the backside of the **die**. The marriage of flip-**chip** bonding and **BGA** leads to FCBGA, an ideal solution for system-on-**chip** devices. This paper outlines the potential application areas of FCBGA, review and analyze the structure and advantages of this **package**, describe the major process flow, present the key technologies used in FCBGA, and address the reliability issues with some encouraging results from current development programs at Fujitsu.

Subfile: B

24/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

5981072 INSPEC Abstract Number: B9809-0170J-011

Title: An EPBGA alternative

Author(s): Karnezos, M.
Author Affiliation: Signetics KP, San Jose, CA, USA

Journal: Advanced Packaging vol.7, no.5 p.90, 92, 94, 96
Publisher: IHS Publishing Group,
Publication Date: June 1998 Country of Publication: USA
ISSN: 1065-0555
SICI: 1065-0555(199806)7:5L.90:EA;1-U
Material Identity Number: F109-98003
Language: English

Abstract: Cavity-up plastic **ball** **grid** array **packages** (**PBGA**) with a two-layer PCB substrate have the lowest cost but have limited thermal and electrical performance. Versions with a four-layer substrate, called enhanced **PBGAs** (EPBGA), provide higher power dissipation (up to 4 W) with additional power and ground planes for shorter routes and lower noise and electrical parasitics, but their cost is significantly greater. Also, although routing more than five rows of solder bumps at 1.27 mm pitch requires more layers, only marginally improved thermal performance is achieved. Cavity-down **BGAs** generally provide higher performance (and higher cost) compared to their cavity-up counterparts. They consist of an integral **spreader** for better **heat** dissipation and a multilayer substrate with power and ground planes for low noise/parasitics. The **die** is mounted in the cavity and **wire** **bonded** to the substrate, followed by **encapsulation**.
The **die** and solder bumps are arrayed on the bottom of the **package** and compete for the same surface area. For this reason, cavity-down **BGAs** (particularly smaller-body versions) cannot accommodate the larger **die** sizes possible in cavity-up **PBGAs**.
There are numerous other differences among the various cavity-down **BGAs** that also can affect performance and cost and depend on the substrate and **heat** **spreader** choice. In this article, the design, construction, performance and advantages of a tape **ball** **grid** array (TBGA) with a single metal layer flex substrate and a

ground plane with laminated **heat spreader** are proposed as an alternative.
Subfile: B

24/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

5953240 INSPEC Abstract Number: B9808-0170J-027
Title: Integrated solutions to bonding **BGA packages** : capillary, wire, and machine considerations
Author(s): Christie, L.; Levine, L.; Eshelman, M.
Author Affiliation: Front Line Process Eng., AMKOR Electron., Chandler, AZ, USA
Conference Title: Proceedings. 1997 International Symposium on Microelectronics (SPIE vol.3235) p.272-7
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA
Publication Date: 1997 Country of Publication: USA xvii+707 pp.
ISBN: 0 930815 50 5 Material Identity Number: XX98-00801
Conference Title: Proceedings 1997 International Symposium on Microelectronics
Conference Sponsor: IMAPS - Int. Microelectron. & Packaging Soc
Conference Date: 14-16 Oct. 1997 Conference Location: Philadelphia, PA, USA
Language: English
Abstract: **Ball grid** array **packages** (**BGAs**) present unique challenges to the **wire bonding** process. They are fine pitch, require long low loops with adequate clearance over voltage and ground bus bar **rings** , and are built on a laminate substrate. A combined approach, encompassing upgraded **wire bonders** and specially designed bonding tools and **bonding wire**, provides a unique opportunity to develop integrated solutions to these technical challenges. A multi-disciplined team is able to drive the optimization process further and faster than groups that only focus on smaller areas of the process. In K&S applications labs located in Pennsylvania, Singapore, and Israel, engineers and customers have worked together to develop solutions that provide robust, high-yield processes. This paper describes the designed experiments (DOEs) and developments that have led to the development of high-yield **BGA** manufacturing processes.
Subfile: B

24/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

5704141 INSPEC Abstract Number: B9711-0170J-031, C9711-7410D-013
Title: Electrical characterization of **BGA packages**
Author(s): Mattei, C.; Agrawal, A.P.
Author Affiliation: Amkor Electron. Inc., Chandler, AZ, USA
Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.1087-93
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 1294 pp.
ISBN: 0 7803 3857 X Material Identity Number: XX97-01595
U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00

Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: For critical high speed applications, system designers budget electrical performance for each individual component within the integration. During the budgeting process, each component is treated as a black box, and is assigned target performance levels. Crosstalk and switching noise levels are specified and closely watched, since they can cause episodes of false switching. SPICE simulations are performed at the **IC**, **package** , and system level to track down any signal integrity problems or issues. Obtaining accurate **package** models, in particular for power and ground, are the key to overall simulation accuracy. **Package** power and ground inductance plays a major role in determining switching noise performance. **Ball Grid** Array (**BGA**) **packages** are constructed with laminate substrates that provide an efficient means for achieving minimal power and ground inductance implementation. A **BGA** that is strategically designed will yield further enhancements in crosstalk and switching noise performance. This is accomplished by optimal implementation and location of power, ground, and signal networks. By doing so, loop inductance created at critical locations in the **BGA** are reduced by mutual inductance. **BGA packages** use power and ground **rings** to provide low inductance access from **Integrated Circuit** (**IC**) bond pads to **package** planes. These connections are typically done using many **bond wires** equally distributed around the perimeter of the **die**. **Rings** are used in combination with via holes, planes, and solder balls to complete the power and ground network structures. Careful attention to how the currents flow in these structures in conjunction with signal traces will yield minimal effective inductance. This paper presents a characterization methodology for creating **BGA** electrical models. It addresses a class of **BGAs** that **contain** power and ground planes, and the Plastic **BGA package** is used as a vehicle. The measurements are performed in frequency domain using a vector network analyzer. Using these models, electrical performance of **BGA packages** is evaluated.
Subfile: B C

24/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

5673403 INSPEC Abstract Number: B9710-0170J-013
Title: New high thermal conductivity thermoplastics for power applications
Author(s): Dietz, R.L.; Peck, D.; Robinson, P.J.; Firmstone, M.G.; Bartholomew, P.M.; Paterson, G.
Author Affiliation: Diemat Inc., Topsfield, MA, USA
Journal: Soldering & Surface Mount Technology vol.9, no.2 p.55-7
Publisher: MCB University Press,
Publication Date: July 1997 Country of Publication: UK
CODEN: SSMOEO ISSN: 0954-0911
SICI: 0954-0911(199707)9:2L.55:HTCT;1-U
Material Identity Number: B310-97002
Language: English
Abstract: The trend towards higher density, higher frequency, higher

power active devices is placing increasingly difficult demands on device **packaging** . Materials with high thermal conductivities are replacing the traditional ceramics in hermetic, high power **packages**, and MCM/hybrid modules. This paper describes the development, properties and application of electrically conductive thermoplastic adhesive pastes having thermal conductivity values as high as 35 W/mK, and able to produce thin, void-free **bond lines** for maximum thermal transfer. The key material variables are isolated and evaluated for their impact of the k value. DOEs (design of experiments) were run to optimise the combination of the key variables, namely size/shape of the filler and the volume fraction to produce the highest k without sacrificing other functional properties such as adhesion. The effect of polymer chemistry (thermoset and thermoplastic) was also studied. The properties of the newly developed, enhanced conductivity thermoplastic adhesives are compared with other material technologies and examples of current applications reviewed.
Subfile: B

24/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

5558526 INSPEC Abstract Number: B9705-5270D-040
Title: A low-cost phased array antenna **packaging** technology
Author(s): Noll, T.E.; Jayaraj, K.; Farrell, B.; Perkins, T.; Glynn, D.
Author Affiliation: Foster-Miller Inc., Waltham, MA, USA
Conference Title: Proceedings of the 1996 Antenna Applications Symposium p.1-18
Publisher: Univ. Massachusetts, Amherst, MA, USA
Publication Date: 1996 Country of Publication: USA vi+508 pp.
Material Identity Number: XX96-02546
Conference Title: Proceedings of 1996 Antenna Applications Symposium
Conference Sponsor: U.S. Air Force; Air Force Mater. Command; Rome Lab.; Hanscom Air Force Base; Antenna Lab.; Univ. Massachusetts; et al
Conference Date: 18-20 Sept. 1996 Conference Location: Monticello, IL, USA
Language: English
Abstract: This paper describes a generic low cost phased array antenna **packaging** technology that uses a highly impermeable liquid crystal polymer (LCP) substrate in multichip module substrate with aperture-coupled patch antennas. Our technology offers a cost-effective approach for fabricating phased array transmitter and receiver modules. The approach has a number of advantages over other conventional approaches, including: (1) low thermal impedance achieved by attaching devices directly to a CTE-matched, high-conductivity **heat sink**; (2) efficient, easy to fabricate slot-coupled RF feeds combined with a high-density flex circuit-based interconnection; (3) excellent electrical performance up to 40 GHz due to the low dielectric constant (2.6 at 1 GHz), and low loss tangent of the LCP; (4) high-sensitivity low-noise performance with LNAs directly connected to antenna elements; (5) low-cost MCM-L processing methods. This **packaging** technology is very flexible and compatible with a wide variety of **chip** and **package** assembly techniques such as **wire bonding** and perimeter/**ball grid** array SMT and is especially suited for direct **chip** attachment using flip **chip** bonding methods. The paper describes preliminary results on a patch antenna fabricated from the LCP substrate, showing 6 dB gain in the Ku-band application area, and on the low cost MCM-1 processing methods used. This technique will enable efficient, large area flat antenna

structures to be fabricated with this innovative MCM-based module approach.
Subfile: B

24/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

5490051 INSPEC Abstract Number: B9703-0170J-032
Title: Two metal layer tape for TAB **ball grid** array
Author(s): Tanaka, H.; Takahashi, G.; Okabe, N.
Author Affiliation: Hitachi Cable Ltd., Ibaraki, Japan
Conference Title: SMI. Surface Mount International. Advanced Electronics Manufacturing Technologies. Proceedings of The Technical Program Part vol.1 p.27-34 vol.1
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 1996 Country of Publication: USA 2 vol. 826 pp.
Material Identity Number: XX96-02550
Conference Title: Proceedings of Surface Mount International. Advanced Electronic Manufacturing Technologies
Conference Sponsor: Electron. Ind. Assoc.; Inst. Interconnecting & Packageing Electron. Circuits; Surface Mount Technol. Assoc.; Miller Freeman
Conference Date: 10-12 Sept. 1996 Conference Location: San Jose, CA, USA
Language: English
Abstract: With recent trends for increasing LSI I/O count and clock speed, the development and practical applications of **ball grid** array (**BGA**) **packages** are becoming more active. Currently, plastic **BGA** (**PBGA**) is the leading **package** in this field, but it is expected that tape **BGA** (TBGA) using TAB tape as an **interposer** will become increasingly important as a technology which can realize a higher I/O count and smaller size **package** at low cost due to its capability for higher circuit density than that of the PCB used as the **interposer** in **PBGA** and for finer pitch **bonding** than **wire bonding**. It is considered that TBGA is also advantageous for high speed devices because of the shrinkage of wiring length due to its higher circuit density. However, a two metal layer TAB tape with a signal/power layer and a ground plane layer on either side of a dielectric film, which produces better electrical properties, is strongly required for a high performance TBGA **package**. We have studied an advanced process for two metal layer TAB tape manufacturing. In this paper, the outline of the results, including new laser technology for via formation and a new copper plating method for via metallization, are described.
Subfile: B

24/3,AB/18 (Item 18 from file: 2)
DIALOG(R)File 2:INSPEC

5438904 INSPEC Abstract Number: B9701-2250-031
Title: A low-cost near-hermetic multichip module based on liquid crystal polymer dielectrics
Author(s): Noll, T.E.; Jayaraj, K.; Farrell, B.; Larmouth, R.S.
Author Affiliation: Foster-Miller Inc., Waltham, MA, USA

Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2794 p.385-90
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1996 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1996)2794L.385:CNHM;1-G
Material Identity Number: C574-96169
Conference Title: 1996 International Conference on Multichip Modules
Conference Sponsor: SPIE; Int. Microelectron. Soc.; Int. Electron. Packging Soc.; et al
Conference Date: 17-19 April 1996 Conference Location: Denver, CO, USA
Language: English
Abstract: This paper describes a generic low cost multichip module technology that uses a highly impermeable liquid crystal polymer (LCP) both as a MCM-L substrate material and as part of a near-hermetic assembly to bring electrical I/O out while providing a thermal management path. The approach has a number of advantages over other conventional approaches, including: (1) homogeneous self-reinforcing dielectrics with very low moisture absorption and excellent dimensional stability, available in any thickness from 25 mu m upwards, with laminated Cu foil of any thickness required; (2) good thermal expansion match throughout the **package** to minimize stresses during assembly and operation; (3) low thermal impedance achieved by attaching devices directly to a CTE matched high conductivity **heat sink**; (4) excellent electrical performance up to microwave frequencies due to the low dielectric constant (<3 at 1 GHz), and low loss tangent of the LCP; and (5) completely compatible with low-cost MCM-L processing methods as well as higher density via forming using plasma or laser drilling. This **packaging** technology is very flexible and compatible with a wide variety of **chip** and **package** interconnection techniques such as **wire bonding** and perimeter/ **ball grid** array SMT and is especially suited for direct **chip** attachment using flip **chip** bonding methods. This paper describes the fabrication and testing of a six-layer MCM-L with application in high speed data processing.
Subfile: B

24/3,AB/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC

5430606 INSPEC Abstract Number: B9701-0170J-057
Title: Flex tape **ball grid** array
Author(s): Karnezos, M.; Goetz, M.; Dong, F.; Ciaschi, A.; Chidambaram, N.
Author Affiliation: ASAT Inc., Palo Alto, CA, USA
Conference Title: 1996 Proceedings. 46th Electronic Components and Technology Conference (Cat. No.96CH35931) p.1271-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 1311 pp.
ISBN: 0 7803 3286 5 Material Identity Number: XX96-01869
U.S. Copyright Clearance Center Code: 0 7803 3286 5/96/$4.00
Conference Title: 1996 Proceedings 46th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 28-31 May 1996 Conference Location: Orlando, FL, USA

Language: English
Abstract: Flex Tape **Ball Grid** Array (FTBGA) is a family of cavity down **BGAs**. The **die**, the flex tape and the solder balls are attached to the bottom side of a metallic heatspreader that acts as the **stiffener** and carrier of the **package**. The **die** is **wire bonded** to the tape traces and then **encapsulated**. The thermal and electrical performance and reliability are clearly superior to the alternative Plastic **Ball Grid** Arrays (**PBGAs**), the conventional plastic and thermally enhanced QFPs. The **packages** are constructed from materials that are well established in the industry. They are assembled using the same equipment, tools and processes as for the assembly of **PBGAs**.
Subfile: B

24/3,AB/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

5362660 INSPEC Abstract Number: B9610-0170J-041
Title: **BGA** performance characteristics: a user's design guide
Author(s): Tarter, T.S.; Goetz, M.P.; Papageorge, M.
Author Affiliation: Adv. Micro Devices Inc., Sunnyvale, CA, USA
Conference Title: SMI Surface Mount International. Advanced Electronics Manufactuting Technologies. Proceedings of the Technical Program p. 245-54
Publisher: SMTA, Edina, MN, USA
Publication Date: 1995 Country of Publication: USA 1082 pp.
Material Identity Number: XX96-01150
Conference Title: Proceedings of Surface Mount International Conference
Conference Date: 29-31 Aug. 1995 Conference Location: San Jose, CA, USA
Language: English
Abstract: The popularity of array **packages**, especially **ball grid** array (**BGA**) formats, is increasing rapidly. Benefits of the **BGA** format include ease of surface mounting due to relaxed lead pitch, relatively low cost, and enhanced performance options. Due to the multitude of **BGA package** styles, many users are unsure which **package** is best suited for specific applications. This paper describes **BGA package** options and the advantages and disadvantages of various styles. The performance specifications consider **BGA** capabilities in terms of thermal and electrical characteristics, as well as measured parameters and theoretical models. **BGA** thermal characteristics vary with **package** style and application environment. Electrical parameters can be designed in while taking into account cost and manufacturability. Performance capabilities of various formats are compared with reference to cost, applicability, and infrastructure for assembly and rework. Physical representations are included for current **BGA** types including overmolded plastic (**PBGA**), cavity plastic (CPBGA), ceramic (CBGA), and tape (TBGA) types. **Die** mounting and **die**-to-**package** interconnects are investigated with emphasis on flip-**chip** and **wire-bond** processes as well as applications for few-**chip** or multichip modules using **BGA** formats. Performance enhancements include internal and external **heat sinking**, power planes in the **BGA** substrate as well as the mounting surface, and signal routing effects. This work aims to help the **package** user select **packages** based on performance and cost and to increase understanding of internal and external effects on **BGA package**

performance.
Subfile: B
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24/3,AB/21 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC

5362657 INSPEC Abstract Number: B9610-0170J-038
Title: An enhanced performance low cost **BGA package**
Author(s): Marrs, R.; Molnar, R.; Lynch, B.; Mescher, P.; Olachea, G.
Author Affiliation: Amkor Electron. Inc., Chandler, AZ, USA
Conference Title: SMI Surface Mount International. Advanced Electronics Manufactuting Technologies. Proceedings of the Technical Program p. 214-25
Publisher: SMTA, Edina, MN, USA
Publication Date: 1995 Country of Publication: USA 1082 pp.
Material Identity Number: XX96-01150
Conference Title: Proceedings of Surface Mount International Conference
Conference Date: 29-31 Aug. 1995 Conference Location: San Jose, CA, USA
Language: English
Abstract: This paper reviews a new class of low-cost, thermally and electrically superior, low profile **ball grid** array **packages** called superBGAs (SBGAs), suitable for both low and high I/O applications. SBGAs are tooled in standard JEDEC outlines ranging from 20-680 balls in 7-50 mm body sizes. The SBGA thermal performance is achieved by incorporation of a **heatsink covering** the **package** top surface and a novel method for efficient heat transfer to all of the solder balls. **ICs** are directly attached to the heatsink in a **die**-down configuration, resulting in maximum **heat spreading** . The enhanced SBGA electrical performance is achieved by design features such as low-inductance conductor paths, microstrip signal lines, efficient power and ground planes, short conductor paths, close proximity power and ground buses to which **wire bonds** are directly connected, and routing of all signal lines without use of vias or through-holes. Also, SBGAs have very good EMI shielding. The topside of the **package** is 100% shielded, and the grid-like solder ball structure provides effective side shielding. The SBGA's design and materials selection has resulted in significantly improved reliability. Advancements have enabled major upgrades in moisture and delamination resistance, solder ball fatigue resistance and reduction in both **chip** and bondwire stress. The **package** consistently demonstrates JEDEC Level 2 (85 degrees C/60%RH/168 hr) preconditioning performance (sufficient for 1 year factory floor life without baking). This paper includes an overview of the **package** structure, materials, manufacturing process, thermal performance, electrical characteristics and reliability.
Subfile: B
Copyright 1996, IEE

24/3,AB/22 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC

5237129 INSPEC Abstract Number: B9605-0170J-136
Title: Recent technology breakthroughs achieved with the new SuperBGA **package**

Author(s): Marrs, R.; Molnar, R.; Lynch, B.; Mescher, P.; Olachea, G.
Author Affiliation: Amkor Electron. Inc., Chandler, AZ, USA
Conference Title: Proceedings of the 1995 International Electronics Packaging Conference p.565-76
Publisher: Int. Electron. Packaging Soc, Wheaton, IL, USA
Publication Date: 1995 Country of Publication: USA 826 pp.
Material Identity Number: XX95-02143
Conference Title: Proceedings of 1995 International Electronics Packaging Conference
Conference Sponsor: Int. Electron. Packaging Soc
Conference Date: 24-27 Sept. 1995 Conference Location: San Diego, CA, USA
Language: English
Abstract: This paper reviews a new class of low-cost, thermally and electrically superior, low profile **ball grid** array **packages** called SuperBGAs. The **packages** are suitable for both low and high I/O applications. The superior thermal performance of SuperBGAs is achieved through incorporation of a **heatsink covering** the entire top surface of the **package** and a novel method of efficiently transferring heat to all of the solderballs. An **IC chip** is directly attached to the heatsink in a "**die** down" configuration, resulting in maximum **heat spreading**. SuperBGA`s enhanced electrical performance is achieved through utilization of a number of design features. These include low-inductance conductor paths, microstrip configuration signal lines, efficient power and ground planes, short conductor paths, close proximity power and ground buses to which **wire bonds** are directly connected, and routing of all signal lines without use of vias or through-holes. Also, SBGAs have very good EMI shielding, a factor critical for today`s portable computers and communication devices. This paper includes an overview of the **package** structure, materials, manufacturing process, thermal performance, electrical characteristics and reliability.
Subfile: B

24/3,AB/23 (Item 23 from file: 2)
DIALOG(R)File 2:INSPEC

4776050 INSPEC Abstract Number: B9411-0170J-024
Title: Capturing design advantages of **BGAs**
Journal: Surface Mount Technology vol.8, no.3 p.36-7, 43
Publication Date: March 1994 Country of Publication: USA
ISSN: 0893-3588
U.S. Copyright Clearance Center Code: 0893-3588/94/$1.00+50
Language: English
Abstract: The construction of the over-molded pad array carrier (OMPAC) begins with a single-layer BT resin epoxy PCB. The **die** is attached via a gold-plated **die** attach and a silver-filled epoxy. Conventional plastic transfer molding **encapsulated** the **package** and interconnection between **die** and epoxy PCB is through thermosonic gold **wire bonding** . From there copper traces are routed to an array of metal pads on the bottom side of the board to which solder bumps (62 Sn, 36 Pb, 2 Ag) are partially reflowed, providing the **package** with 'leads.' For increased heat dissipation, OMPACs include thermal vias (copper plated-through holes) directly beneath the **die**. Copper foil serves to **distribute** the **heat** to specific solder balls, which are connected to the system PCB (product) ground plane(s).

Subfile: B

24/3,AB/24 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05818729
E.I. No: EIP01216511369
Title: Integrated transient thermal and mechanical analysis of molded **PBGA packages** during thermal shock
Author: Mercado, L.L.; Lee, T.Y.; Cook, J.
Corporate Source: Interconnect Systems Laboratories Motorola, Inc., Tempe, AZ 85284, United States
Source: IEEE Transactions on Advanced Packaging v 24 n 1 February 2001 2001. p 66-75
Publication Year: 2001
CODEN: ITAPFZ ISSN: 1521-3323
Language: English
Abstract: During thermal shock, large thermal gradients exist within a molded plastic **ball grid** array (**PBGA**) **package**. The conventional assumption of uniform temperature distribution becomes invalid. In this paper, an integrated thermal-mechanical analysis was performed to evaluate the transient effect of thermal shock. For comparison, an isothermal analysis was also conducted. The computational fluid dynamics (CFD) method was used to obtain the thermal boundary conditions surrounding the **package**. The heat transfer coefficient obtained through CFD was compared to two analytical solutions. It was found that the analytical values were not acceptable in the time period of interest. Therefore, to obtain the actual maximum **die** stress, CFD solution has to be used instead of analytical solutions to derive the thermal boundary condition. This boundary condition was then applied to the **package** and a sequentially coupled heat transfer and thermal stress analysis was performed. The transient analysis has shown that high stresses occur in the **die** due to thermal shock, which can not be seen under the traditional isothermal assumption. The impact of plastic **ball grid** array (**PBGA**) **package** parameters on transient **die** stress was also studied, including mold thickness and substrate thickness. The results in this paper could be applied to either **wire bond** or flip-**chip PBGA packages**. 12 Refs.

24/3,AB/25 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04385850
E.I. No: EIP96043148163
Title: Technology driven component **package** trends
Author: Prasad, Ray
Corporate Source: Ray Prasad Consultancy Group, Portland, OR, USA
Source: Semiconductor International v 19 n 4 Apr 1996. 6pp
Publication Year: 1996
CODEN: SITLDD ISSN: 0163-3767
Language: English
Abstract: Surface mount technology has matured to the point that it is the technology of choice for modern electronics products. It has also evolved from through-hole to fine pitch, ultra-fine pinch, **BGA**,

chip scale and finally to direct **chip** attach. To accommodate higher pin counts, the lead pitches have been dropping. As lead pitches have dropped, problems in design and manufacturing with the fine and ultra-fine pitch **packages** have increased. To alleviate some of the manufacturing problems, newer **packaging** technology are being used. However, there is no real technology hurdle in the widespread use any **packages** because technical details of TAB, **wire bond**, flip **chip**, and CSP are well known to the industry.

24/3,AB/26 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04127293
E.I. No: EIP95042656559
Title: MBGA
Author: Anon
Source: Circuits Assembly v 6 n 3 Mar 1995. p 68
Publication Year: 1995
CODEN: CIATE5 ISSN: 1054-0407
Language: English
Abstract: In a single-layer metal **ball grid** array (MBGA) **package**, a thin-film metal circuit layer is deposited on an anodized aluminum substrate. After **die** attach and **wire bond**, the cavity is filled with an **encapsulant**, and eutectic solder balls are attached. The MBGA **package** provides reliable performance in a size suitable for many applications. The aluminum substrate acts a **heat sink** that greatly reduces thermal resistance, a feature not found in any other **BGA** technology. Overall, the MBGA **package** is a low-cost and high-performance product in terms of electrical performance and routability.

24/3,AB/27 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04494427 JICST ACCESSION NUMBER: 00A0178862 FILE SEGMENT: JICST-E
Development of TBGA(Tape **Ball Grid** Arey) for Media Processor.
OTAKA TATSUYA (1); SUGIMOTO HIROSHI (1); OMORI TOMOO (1); SUZUKI SACHIO (1)
(1) Hitachi Cable, Ltd., System's Material Lab., JPN
Hitachi Densen, 2000, NO.19, PAGE.79-84, FIG.10, TBL.7, REF.5
JOURNAL NUMBER: Y0197AAZ ISSN NO: 0910-2817
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.75
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

24/3,AB/28 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03887374 JICST ACCESSION NUMBER: 98A0788083 FILE SEGMENT: JICST-E
CSP/**BGA** advancing in adoption and circuit/**packaging** design technology. BCC for fewer pins of Fujitsu Ltd., and its reliability evaluation and characteristics. Adoption of **interposer**-less

structure in which mounted terminals are arranged peripherally around the device, for realization of improvement of various characteristics and reduction of the mounting area.
SAKODA HIDEHARU (1)
(1) Fujitsu Ltd.
Denshi Gijutsu(Electronic Engineering), 1998, VOL.40,NO.11, PAGE.25-29, FIG.15, REF.7
JOURNAL NUMBER: F0571AAK ISSN NO: 0366-8819 CODEN: DEGIA
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The titled BCC (Bump **Chip** Carrier) is explained. A mounted terminal of BCC is of resin bump structure having a metal plating film on base of resin. It is of **interposer**-less structure applying **wire bonding** technique for joint of bump and device. This paper explains the manufacturing processes, leadframe tehcnique developed for realization of resin bump, etc. Reflow-proof crack reliability of BCC for 48 pins under development was investigated, and it was known that there was no problem because of its simple structure.

24/3,AB/29 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02267163 JICST ACCESSION NUMBER: 94A0779437 FILE SEGMENT: JICST-E
Special issue : New-type **packages** and problems of **packaging** technology. Features of substrates for P-**BGA**.
KATO YOJI (1); HARA KAORU (1)
(1) Eastern Co., Ltd.
Denshi Zairyo(Electronic Parts and Materials), 1994, VOL.33,NO.9, PAGE.44-48, FIG.14, REF.2
JOURNAL NUMBER: F0040AAH ISSN NO: 0387-0774
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper explains the features and the future problems of the substrates for the plastic **ball grid** array. This paper describes that bismaleimide and triazine series resin are used as the substrate materials in view of the heat resistance, and explains that the double-sided board, the multi-layer board, and the step type structure multi-layer board, regarding to its structures. The connection between the **ICs** and the substrates by the **wire bonding** is also explained.

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SYSTEM:OS  - DIALOG OneSearch
  File 350:Derwent WPIX  1963-2001/UD,UM &UP=200209
        (c) 2002 Derwent Info Ltd
*File 350: Price changes as of 1/1/02. Please see HELP RATES 350.
More updates in 2002.  Please see HELP NEWS 350.
  File 347:JAPIO  Oct/1976-2001/Oct(Updated 020204)
        (c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.

Set     Items   Description
S1       5652   BALL()GRID? ? OR BALLGRID? OR BGA OR BGAS OR PBGAS OR PBGA
            OR CGA OR CGAS
S2       7484   (SOLDER OR SOLDERING OR SOLDERED OR BRAZ?)(2N)(BALL OR BAL-
            LS OR PADS OR PAD OR SPHERE? ?)
S3     128118   (HEAT? OR WARM? OR HOT? ? OR THERMOL? OR THERMAL? OR PREHE-
            AT? OR MELT? OR FUSE? ? OR FUSING? ? OR FUSION?)(3N)(SPREAD?
            OR CIRCULATE? OR DISPERS? OR DISTRIBUT? OR RADIAT? OR SCATTER?
             OR COVER? OR OVERLAY?)
S4       4882   ((HIGH?? OR HEIGHTEN? OR RAIS? OR INCREAS? OR ELEVAT?)(2N)-
            (TEMP? ? OR TEMPERATUR?))(3N)(SPREAD? OR CIRCULATE? OR DISPER-
            S? OR DISTRIBUT? OR RADIAT? OR SCATTER? OR COVER? OR OVERLAY?)
S5     124403   (CIRCUIT)(2N)(BOARD? ?) OR (SYSTEM? ?()BOARD? ?) OR MOTHER-
            BOARD?
S6     151293   SOLDER OR SOLDERING OR SOLDERED OR BRAZ?
S7        488   MC=V04-R06D3
S8     848200   IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT? ?)) OR (MI-
            CRO)(W)(CIRCUIT? ? OR CHIP? ? OR ELECTRONIC?) OR CHIP? ? OR M-
            ICROCIRCUIT? ? OR DIE? ? OR LOGIC(W) CIRCUIT? ? OR WAFER? ? OR
             MICROELECTRONIC?
S9      21835   (CONTACT? OR BONDING)(2N)(PAD OR PADS OR BUMP OR BUMPS)
S10     32085   (WIRE OR WIRES OR LINE OR LINES)(2N)(BOND?)
S11      6606   MC=U11-E01A
S12     51780   IC=(H01L-021/60 OR H01L-021/603 OR H01L-021/607)
S13      3797   (CONDUCTIV?)(3N)(BUMP? OR PAD OR PADS)
S14   4417385   ENCLOS??? OR HOUS??? OR CASE? ? OR CONTAIN? OR ENCASE? OR
            ENCAPSUL? OR PACKAG?
S15    202761   (S1 OR S8) AND S14
S16      3885   S1 AND S14
S17      1149   S16 AND S2
S18       223   S17 AND S5
S19         7   S18 AND (S3 OR S4)
S20        38   S17 AND (S3 OR S4)
S21        31   S20 NOT S19
S22    632458   HEAT?()SINK? OR RING? ? OR INTERPOSER? OR STIFFENER?
S23       310   S16 AND S22
S24        81   S23 AND S2
S25        20   S24 AND S5
S26        20   S25 NOT (S19 OR S21)
S27       309   S8 AND S1 AND S14 AND (S3 OR S4 OR S22)
S28        35   S27 AND S9
S29        26   S28 NOT (S19 OR S21 OR S26)
S30        10   S27 AND S13
S31         6   S30 NOT (S19 OR S21 OR S26)
S32         9   S29 AND (S10 OR S11)
S33        19   S30 OR S32
S34         8   S33 NOT S29
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S35 19 S33 OR S34

? T S19/3,AB/1-3

19/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012299232
WPI Acc No: 1999-105338/199909
XRPX Acc No: N99-076071
Integrated circuit **package** for **BGA** - has **heat spreader** which is coupled to IC die using thermally conductive adhesive and has area larger than die cavity
Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: RILEY J B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5856911	A	19990105	US 96747347	A	19961112	199909	B

Priority Applications (No Type Date): US 96747347 A 19961112
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5856911	A		6	H05K-007/20	

Abstract (Basic): US 5856911 A
The **package** (28) has a top cavity (30) for holding an IC die (32). The cavity is formed in a planar laminate material (29). The die is bonded with bond wires (34) to electrical traces on top of the laminate material and coupled through electrical vias to **solder balls** (36).
A **heat spreader** (38) is connected to the die using a thermally conductive adhesive and has an area larger than the cavity. A thermally conductive slug (40) is coupled to the **heat spreader** and spans through an opening (44) formed in the **circuit board** (28) where the **package** is placed.
USE - For PGA, SPGA.
ADVANTAGE - Maintains mechanical and thermal compatibility with existing design for TCP circuit layer. Facilitates installation and requires only standard **BGA** manufacturing equipment. Raises yield rate.
Dwg.2/5

19/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012202796
WPI Acc No: 1999-008902/199901
XRPX Acc No: N99-006376
Single tier semiconductor **package** e.g. **PBGA**,CBGA - has lid arranged covering **encapsulant** for limiting height of **encapsulant** protruding from lower surfaces of **package** substrate
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: MERTOL A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5834839	A	19981110	US 97861884	A	19970522	199901	B

Priority Applications (No Type Date): US 97861884 A 19970522
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5834839	A		6	H01L-023/12	

Abstract (Basic): US 5834839 A

The **package** includes a single tier **package** substrate (303) with a central hole. Electrical contacts on lower surface (303b) of the **package** substrate are connected to the electrical contacts on a printed **circuit board** (301). A **heat spreader** (307) **covers** one side of the central hole when attached to an upper surface (303a) of the **package** substrate. A semiconductor die (304) is attached to the **heat spread** inside the central hole and electrically connected to the electrical contacts on the lower surface of the **package** substrate. An **encapsulant** (308) covers the semiconductor die inside the central hole. A lid (300) is arranged covering the **encapsulant** for limiting the height of the **encapsulant** protruding from the lower surface of the **package** substrate.

ADVANTAGE - Extends life and reduces failure rate of devices by facilitating thermal dissipation. Preserves clearance between **encapsulant** and printed **circuit board**. Improves tensile strength and heat transfer capability of lid. Protects delicate bond wiring by quick heat dissipation. Improves mechanical strength and deformation resistance of **solder balls**.

Dwg.3A/4

19/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06244862
PLASTIC **CIRCUIT BOARD**

PUB. NO.: 11-186436 [JP 11186436 A]
PUBLISHED: July 09, 1999 (19990709)
INVENTOR(s): FUKUNAGA NORIKAZU
APPLICANT(s): SUMITOMO METAL SMI ELECTRON DEVICES INC
APPL. NO.: 09-350729 [JP 97350729]
FILED: December 19, 1997 (19971219)

ABSTRACT

PROBLEM TO BE SOLVED: To improve **heat radiation** of a plastic **circuit board**.

SOLUTION: An IC chip 12 is loaded on a plastic **circuit board** 11, and molded by sealing resin 14, and plural **solder balls** 15 are joined to the lower face of the plastic **circuit board** 11 so that a **PBGA package** 10 can be constituted. A conductive pattern is formed of copper foil or the like on the both faces of the plastic **circuit board** 11. The area ratio of a conductive pattern 16 to the board area is 60% or more, and preferentially, 80% or more. The conductive pattern is formed so that all boundary parts between the adjacent conductive patterns can be thin wires whose thin width is 80 μm (that is, line width which is absolutely necessary for insulation between

the conductive patterns). Thus, heat resistance of the plastic **circuit board** 11 as a whole can be reduced, and the **heat radiation** of an IC chip 12 can be efficiently attained in a path from the plastic **circuit board** 11 to a printed **circuit board** 19.

19/3,AB/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06156024
CAVITY-DOWN TYPE **BGA PACKAGE**

PUB. NO.: 11-097567 [JP 11097567 A]
PUBLISHED: April 09, 1999 (19990409)
INVENTOR(s): NAKADA YOSHIKAZU
TAKAMICHI HIROSHI
APPLICANT(s): SUMITOMO METAL SMI ELECTRON DEVICES INC
APPL. NO.: 09-256949 [JP 97256949]
FILED: September 22, 1997 (19970922)

ABSTRACT

PROBLEM TO BE SOLVED: To improve the adhesive force and the **heat radiation** of a plurality of metal plates constituting the **heat-radiation** slug of a cavity-down type **BGA package**.

SOLUTION: A **heat-radiation** 21 is constituted by a planar metal plate 22 and a metal plate 23 having a punched opening for a cavity 24 in the center, these two metal plates 22, 23 being bonded with brazing material 25 such as AgCu. A plastic **circuit board** 26 is bonded to the bottom surface of the **heat- radiating** slug 21 via an adhesive resin sheet 27 and many **solder balls** 28 as connecting electrodes are arranged on the bottom surface of the plastic **circuit board** 26. A semiconductor chip 30 is die-bonded to the cavity 24 of the **heat- radiation** slug 21, the semiconductor chip 30 is connected to the plastic **circuit board** 26 with a bonding wire 31, and then the cavity 24 is filled with sealing resin 32. In this **case** , the metal plates 22, 23 are bonded to each other with brazing material 25 to improve the adhesive force and heat dissipation.

19/3,AB/5 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06126431
BALL GRID ARRAY **PACKAGE**, MANUFACTURE THEREOF AND PRINTED **CIRCUIT BOARD** THEREFOR

PUB. NO.: 11-067968 [JP 11067968 A]
PUBLISHED: March 09, 1999 (19990309)
INVENTOR(s): AN INTETSU
KA YUKI
RI EIBIN
APPLICANT(s): SAMSUNG ELECTRON CO LTD
APPL. NO.: 10-049245 [JP 9849245]
FILED: March 02, 1998 (19980302)
PRIORITY: 9738466 [KR 38466], KR (Korea) Republic of, August 12, 1997 (19970812)

ABSTRACT

PROBLEM TO BE SOLVED: To avoid moisture absorption through **heat**

radiating vias and improve **heat radiation**, by filling these vias with a metal having a high thermal conductivity and low moisture absorption.
SOLUTION: A **package** 200 comprises a printed **circuit board** 110 having a chip mounting region 160 and a circuit pattern 15, a semiconductor chip mounted on the mounting region 160, bonding wires 140 for electrically connecting the semiconductor chip to a circuit pattern 115, a **package** body 150 formed with the sealed semiconductor chip and the bonding wires 140, and **solder balls** 130. **Heat radiating** vias 162a are formed in a lower part of the chip-mounting region 160 to **radiate** out the **heat** generated during operating of the chip and filled with a low-m.p. metal 172 to avoid penetrating the water content in the **package** body, and to improve the **heat radiation**.

19/3,AB/6 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

06062449
THIN-FILM POWER TAPE **BALL GRID** ARRAY **PACKAGE**

PUB. NO.: 11-003957 [JP 11003957 A]
PUBLISHED: January 06, 1999 (19990106)
INVENTOR(s): CHIA CHOK J
VARIOT PATRICK
ALAGARATNAM MANIAM
APPLICANT(s): LSI LOGIC CORP
APPL. NO.: 10-109632 [JP 98109632]
FILED: April 20, 1998 (19980420)
PRIORITY: 840614 [US 840614], US (United States of America), April 21, 1997 (19970421)

ABSTRACT
PROBLEM TO BE SOLVED: To provide a **ball grid** array **package** which is economical and high in its density.

SOLUTION: An integrated circuit **package** 2 includes a **heat spreader** 4 formed to have a central recess face 16 between its flat faces 12 and 14, and also includes flexible tapes extended from the flat faces 12 and 14 to the central recess face 16. A semiconductor chip 24 is mounted on the central recess face 16 between the flexible tapes and then, by wire bonding, the bonding pads of the chip 24 are interconnected to a metal interconnect pattern of the tapes. Then plastic molding or epoxy is applied to seal the chip and wire bonding on the central recess face of the **heat spreader** 4. Thereby the **package** 2 can be easily mounted on a **motherboard** by means of **solder balls**.

19/3,AB/7 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

05842733

BGA TYPE **PACKAGE** MOUNTING SUBSTRATE AND **BGA** TYPE **PACKAGE** MOUNTING METHOD

PUB. NO.: 10-125833 [JP 10125833 A]
PUBLISHED: May 15, 1998 (19980515)
INVENTOR(s): HASEGAWA TAKAHIKO
APPLICANT(s): DENSO CORP [000426] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-280925 [JP 96280925]
FILED: October 23, 1996 (19961023)

ABSTRACT

PROBLEM TO BE SOLVED: To test the solder bond condition using an X-ray, and improve the **heat radiation** power using a metal-made heat dissipation member.

SOLUTION: A **circuit board** 30 has heat dissipation through-holes 34 for transmitting the heat transmitted through **solder balls** 20 from a **BGA**(**ball grid** array) **package** 1 to the substrate back side. The **package** 1 is disposed on the surface of the **circuit board** 30 and soldered by the solder reflow method. The solder bond condition of the board 30 to the **package** 1 is inspected by the X-ray. After the inspection, a heat dissipation member 40 for dissipating the heat transmitted from the through-holes 34 of the board 30 is mounted on the back surface of the board 30.

21/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013728527
WPI Acc No: 2001-212757/200122
Related WPI Acc No: 2001-193334; 2001-212745; 2001-498073
XRAM Acc No: C01-063592
XRPX Acc No: N01-151982

Integrated circuit **ball grid** array **package**, has conductive layers at ground potential formed on opposite sides of signal and power lines to lower self and mutual inductances

Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: JAMES R D; LAMSON M A
Number of Countries: 025 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1079433	A2	20010228	EP 2000117329	A	20000821	200122	B

Priority Applications (No Type Date): US 99151016 P 19990827
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1079433	A2	E	9	H01L-023/498	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Abstract (Basic): EP 1079433 A2
Abstract (Basic):

NOVELTY - High performance integrated circuit (IC) **package** comprises:

(a) a first conductive layer (115) providing ground potential; and

(b) a second conductive layer (105) also at ground potential.

The conductive layers are formed on opposite sides of signal and power lines so that self and mutual inductances are lowered, to reduce **package** electrical noise and cross-talk, and increase circuit switching and speed.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of fabricating a high performance, high I/O **ball grid** array (**BGA**) **package**, which comprises:

(i) providing a substrate (110) having two metal layers (115, 116) and an intermediate insulating layer (113) having metal filled vias (114) in it;

(ii) forming the metal layers such that one (115) provides electrical ground potential, and the other (116) provides electrical signal and power potentials;

(iii) forming protective insulating films (111, 112), usable as solder masks, over the exposed surfaces of the metal layers, of a thickness which reduces electrical inductances of the signal and power lines;

(iv) forming openings (123, 112a) in both insulating films, and filling them with solderable metal to create attachment sites for outside **solder balls** and chip **solder** bumps;

(v) attaching an IC chip (101), having an active surface (101a) including solder bumps (102) and a passive surface (101b), by adhering the solder bumps to the metal filled openings in one of the insulating films (111);

(vi) attaching part of a **heat spreader** to the passive surface;

(vii) attaching the remaining parts of the **heat spreader** to the insulating film (111) using an electrically conductive adhesive (130); and

(viii) attaching **solder balls** (106) to the metal filled openings (112a) in the other insulating film (112).

USE - For high performance **BGA packages** for flip chip assembly.

ADVANTAGE - **Package** electrical noise and cross-talk are reduced, and IC switching and speed are increased.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through the above **BGA package**.

21/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013717045
WPI Acc No: 2001-201269/200120
XRPX Acc No: N01-143375
Flip chip **ball grid package** manufacturing method involves laminating dielectric on top surface of base layer in substrate, such that cavity in dielectric exposes top surface of base layer
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: DESAI K; NAGARAJAN K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6133064	A	20001017	US 99322064	A	19990527	200120	B

Priority Applications (No Type Date): US 99322064 A 19990527
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6133064	A		5	H01L-021/44	

Abstract (Basic): US 6133064 A
Abstract (Basic):

NOVELTY - A dielectric (12) is laminated on top surface (11) of base layer (10) in substrate (8), so that cavity (14) in dielectric exposes top surface. A die (18) is partially placed within cavity and mounted on top surface of base layer, so that active surface (20) of die faces top surface (11). Bond pads (21) in active surface are electrically coupled with **solder balls** (29) on bottom surface (13) of base layer.

DETAILED DESCRIPTION - The substrate has base layer with top and bottom surfaces. The die has active surface and inactive surface (22). The inactive surface has several bond pads. The dielectric is laminated on top surface of base layer with several traces such that upper portion of dielectric forms a frame. A **heat spreader** is placed within the frame such that it rests on dielectric.

USE - For manufacturing flip chip **ball grid** array **package**.

ADVANTAGE - The dielectric layer laminated on top surface of base layer prevents warpage of die and substrate during mounting of die. The frame formed on upper portion of dielectric helps **heat spreader** placement more accurately.

DESCRIPTION OF DRAWING(S) - The figure shows the cross sectional view of flip chip **ball grid** array **package**.

Substrate (8)

Base layer (10)

Top surface of base layer (11)
Dielectric (12)
Bottom surface of base layer (13)
Cavity (14)
Die (18)
Active surface of die (20)
Bond pads (21)
Inactive surface of die.(22)
Solder balls (29)
pp; 5 DwgNo 2/3

21/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013660182
WPI Acc No: 2001-144394/200115
XRAM Acc No: C01-042838
XRPX Acc No: N01-106036
Resin sealed semiconductor **package** includes resin injection hole formed between lower surface of wiring board and upper surface of heat sink such that injected resin reaches upper surface of wiring board
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001007260	A	20010112	JP 99180310	A	19990625	200115	B

Priority Applications (No Type Date): JP 99180310 A 19990625
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001007260	A		7	H01L-023/29	

Abstract (Basic): JP 2001007260 A
Abstract (Basic):
NOVELTY - A resin injection hole (17) for injecting resin is formed between the upper surface of heat sink (7) and lower surface of wiring board (31) mounted on a substrate (1) such that the injected resin (11) reaches upper surface of wiring board and also **covers** surface of **heat** sink. **Solder balls** are then mounted on wiring board.
DETAILED DESCRIPTION - The wiring board in which the wiring pattern is formed, is mounted on substrate so that the semiconductor chip (4) mounted on substrate is surrounded. A bonding wire (5) connects the electrode of semiconductor device and the terminal provided on the wiring board. An INDEPENDENT CLAIM is also included for semiconductor **package** manufacturing method.
USE - Resin sealed semiconductor **package** such as **ball grid** array (**BGA**) **package**.
ADVANTAGE - Since resin injection hole is provided, need for plate for resin injection is eliminated and thus manufacturing process of semiconductor device becomes simple and hence yield of semiconductor device is improved.

21/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013652310
WPI Acc No: 2001-136522/200114
XRPX Acc No: N01-099297
Heat spreader for a ball and grid array **package** with a chip attached to a first surface of a substrate by adhesives uses a substrate with two surfaces with **solder balls** formed on it and soldered to another device
Patent Assignee: CAESAR TECHNOLOGY INC (CAES-N)
Inventor: LI J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6163458	A	20001219	US 99453439	A	19991203	200114	B

Priority Applications (No Type Date): US 99453439 A 19991203
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6163458	A		4	H05K-007/20	

Abstract (Basic): US 6163458 A
Abstract (Basic):

NOVELTY - The **heat spreader** for a ball and grid array **package** with a chip attached to a first surface of a substrate by adhesives uses a substrate with two surfaces with **solder balls** formed on it and soldered to another device. A chip (30) is attached in the cavity (12) in the first surface by adhesive. A **heat spreader covers** the chip, with a protuberance formed on the **heat spreader** contacting the chip.

USE - As a **heat spreader** for a ball and grid array **package** with a chip attached to a 1st surface of a substrate by adhesives.

ADVANTAGE - Protuberances on the **heat spreader** contacts the chip to enhance the heat dissipation effect of the chip.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross sectional view of the **ball grid** array **packaged** device.

21/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013279648
WPI Acc No: 2000-451583/200039
XRPX Acc No: N00-336224
Ball grid array semiconductor device **package** has substrate which includes **solder balls** which are connected to copper stiffener through holes on substrate
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: HASSANZADEH N; KALIDAS N; LAMSON M A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6084777	A	20000704	US 9744173	A	19970423	200039 B
			US 9865670	A	19980423	

Priority Applications (No Type Date): US 9744173 P 19970423; US 9865670 A 19980423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6084777	A		7	H05K-007/20	Provisional application US 9744173

Abstract (Basic): US 6084777 A
Abstract (Basic):
NOVELTY - Copper stiffener (13) is mounted to **heat spreader** (14) provided on substrate (16). **Solder balls** (20) are formed on the stiffener along with holes. A die with several die pads is mounted on the **heat spreader**. The **solder balls** are connected to the stiffener through holes in substrate.
USE - For packing semiconductor devices used in micro electronic mechanical system.
ADVANTAGE - Eliminates the need to form a cavity in a **heat spreader**, thereby overall manufacturing cost is reduced. As stiffener can be used as power plane or ground plane, the overall complexity is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows sectional view of **ball grid** array **package**.
Copper stiffener (13)
Heat spreader (14)
Substrate (16)
Solder ball (20)
pp; 7 DwgNo 2/3

21/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013192417
WPI Acc No: 2000-364290/200031
XRAM Acc No: C00-109842
XRPX Acc No: N00-272620
Integrated circuit **package** e.g. **ball grid** array **package** has flex tape which has conductive metal lead pattern positioned on side of tape facing substrate with apertures, exposes lead

pattern for **solder ball** bonding
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: ALAGARATNAM M; CHIA C J; LOW Q H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6057594	A	20000502	US 97842379	A	19970423	200031	B

Priority Applications (No Type Date): US 97842379 A 19970423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6057594	A		5	H01L-023/495	

Abstract (Basic): US 6057594 A
Abstract (Basic):

NOVELTY - IC **package** has molded plastic base structure sandwiched between heat conductive substrate (4) and flex tape (16). Flex tape has conductive metal lead pattern (18) positioned on tape side facing substrate with apertures (22) that exposes lead pattern for **solder ball** bonding. Semiconductor IC (12) is mounted on central point of **heat spreader** (10). Chip and wiring bonding are then **encapsulated** on substrate.

DETAILED DESCRIPTION - A molded plastic base structure includes heat conductive substrate and flex tape extending from corresponding side of substrate. The heat conductive substrate is laminate structure comprising metal and ceramics. The molded plastic material is present between substrate and flex tape which has conductive metal lead pattern on the tape side which faces the substrate. Apertures exposes conductive lead pattern for **solder ball** bonding. A semiconductor IC chip with active and non-active side is mounted to central portion of **heat spreader** and active side has bond pads (14) for interconnecting integrated circuit. Wire bonding interconnects bond pads on clip to metal lead pattern chip. The wire bonding are then **encapsulated** on substrate by filling cavity in the substrate partially by a resin. The cavity has molded plastic along its side walls. The flex tape also extends along side walls of cavity.

USE - For large scale integrated (LSI) circuits, integrated circuit (IC) **packages** e.g. **ball grid** array (**BGA**) **package**, formed by tape automated bonding (TAB).

ADVANTAGE - As chip is directly fixed to **heat spreader** **heat** dissipation is increased. Wire bonding is lower in cost and has flexibility higher then tape automated bonding (TAB) hence resulting **package** is economical to manufacture, thin and light weight.

DESCRIPTION OF DRAWING(S) - The figure shows perspective view of **ball grid** array **package**.

Heat conductive substrate (4)
Heat spreader (10)
Semiconductor integrated chip (12)
Bond pads (14)
Flex tape (16)
lead pattern (18)
Apertures (22)
pp; 5 DwgNo 3/5

21/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012550752
WPI Acc No: 1999-356858/199930
XRPX Acc No: N99-265644
High performance cavity-down, **ball grid** array **package** for integrated circuit
Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N)
Inventor: HAMZEHDOOST A; MARTIN R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5910686	A	19990608	US 98121792	A	19980723	199930	B

Priority Applications (No Type Date): US 98121792 A 19980723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5910686	A		10	H01L-023/48	

Abstract (Basic): US 5910686 A
Abstract (Basic):
NOVELTY - A die-cavity has an insulating tape projecting into it so that the die can be bonded to the tape. The other end of the tape extends from the cavity so that conductive traces connect the wire bonding sites to solderable areas on the outer area of the tape.

DETAILED DESCRIPTION - The cavity-down HBGA integrated-circuit **package** for an integrated-circuit die, includes:

(1) an integrated-circuit die (112) with a die-mounting surface and a surface which has wire-bonding pads (114) formed on it;

(2) a die-carrier/**heat spreader** (102) which has a die-cavity (104) formed through its lower surface, where the die-mounting surface of the integrated-circuit die is attached to the top interior surface of the die-cavity, and where the die-carrier/**heat spreader** also has a lower surface outside of and surrounding the cavity;

(3) a first portion (122) of an insulated tape layer (120) which extends over the lower outside surface of the die-carrier/**heat spreader** outside of the die-cavity;

(4) the insulated tape layer also has second portions (126) which are located inside the die-cavity of the die-carrier/heat sink and which have wire-bonding sites (132) formed on them;

(5) several bonding-wire loops (140), each of which is looped between and bonded to one of the wire-bonding pads formed on the integrated-circuit die and a respective wire-bonding site formed on the insulated tape layer within the die-cavity to form bonding-wire loops;

(6) conductive traces (134) are formed on the insulated tape layer to connect the wire-bonding sites located inside of the die-cavity to respective selective solderable areas (137) formed on the insulated layer outside of the die-cavity;

(7) where the selective solderable areas on the insulated layer and outside of the die-cavity are arranged in a grid pattern on the bottom side of a die-down HBGA **package**;

(8) several **solder balls** (136) attached to respective selective solderable areas formed on the insulated layer outside of the die-cavity; and

(9) an **encapsulation** layer (150) or cover for covering and sealing the integrated-circuit die, the bonding wires, where the **encapsulation** layer or cover has a lower outside surface formed in it and is spaced apart from a surface to which an HBGA **package** is mounted.

USE - The HBGA is used for integrated circuits.
ADVANTAGE - Minimizes the thickness of the **encapsulating** layer while still accommodating a greater number of bonding wires, providing smaller grid spacing for smaller **solder balls**.
DESCRIPTION OF DRAWING(S) - The drawing shows an enlarged side sectional view of the cavity-down **encapsulated** HBGA **package**

21/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012180204
WPI Acc No: 1998-597117/199851
XRAM Acc No: C98-179352
XRPX Acc No: N98-464724
Thin power tape **ball grid** array **package** - has semiconductor chip mounted in **heat spreader** recess and its bonding pads connected to metal interconnect patterns on flex tape.
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: ALAGARATNAM M; CHIA C J; VARIOT P
Number of Countries: 027 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 880175	A2	19981125	EP 98303039	A	19980421	199851	B
JP 11003957	A	19990106	JP 98109632	A	19980420	199911	
US 5869889	A	19990209	US 97840614	A	19970421	199913	

Priority Applications (No Type Date): US 97840614 A 19970421
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 880175	A2	E	5	H01L-023/13	
JP 11003957	A		4	H01L-023/12	
US 5869889	A			H01L-023/34	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Abstract (Basic): EP 880175 A
Package comprises a heat conductive support (10) formed to have a recessed portion with opposing planar surfaces (12,14) and a centrally disposed surface (16). Flex tape is attached to the planar surfaces (12,14) and extends to the centrally disposed surface (16). The flex tape includes one or more metal interconnect patterns (22) on an exposed surface. Semiconductor integrated circuit chip (24) is mounted on centrally disposed surface (16) spaced from the flex tape (18,20). Chip (24) has bonding pads (26). Wire bonds interconnect pads (26) to the interconnect pattern (22). Preferably chip (24) and the wire bonds are **encapsulated** by plastic molding or epoxy on the heat conductive support (10). Preferably the metal interconnect pattern (22) is connected by **solder balls** to a mother board.
USE - Flex tape **ball grid** array **package** where the flex tape and a formed **heat spreader** provide the **package** substrate.
ADVANTAGE - The use of flex tape for the substrate is cheaper to manufacture than laminates and ceramics and the wire bonding for the interconnect of the chip and the substrate is lower in cost has higher flexibility than other interconnects such as TAB bonding. The recess or cavity for attachment of the chip to the **heat spreader** allows for greater protection of the chip and easier assembly of a thin

and light **package**.

21/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012143341
WPI Acc No: 1998-560253/199848
XRAM Acc No: C98-167831
XRPX Acc No: N98-436911
Ball grid array (**BGA**) **package** for integrated circuits used in e.g. mobile telephones - has a metal **heat** sink **covered** in an insulating sheet including conductive traces, with a central hole into which is mounted the device
Patent Assignee: HYUNDAI ELECTRONICS IND CO LTD (HYUN-N)
Inventor: CHOI K H; JEONG T S; LEE T K; PARK J S; RYU K T; YOUN H S; CHOI K ; JEONG T; LEE T; PARK J; RYU K; YOUN H; CHOI G H; CHUNG T S; LEE T G; RYOO G T; YOON H S
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2325340	A	19981118	GB 986078	A	19980320	199848	B
DE 19821715	A1	19990128	DE 1021715	A	19980514	199910	
CN 1199927	A	19981125	CN 98107932	A	19980506	199915	
JP 11045956	A	19990216	JP 98100428	A	19980327	199917	
KR 98083733	A	19981205	KR 9719144	A	19970517	200007	
KR 98083734	A	19981205	KR 9719145	A	19970517	200007	
US 6060778	A	20000509	US 9860981	A	19980415	200030	
KR 220249	B1	19990915	KR 9719144	A	19970517	200107	

Priority Applications (No Type Date): KR 9719145 A 19970517; KR 9719144 A 19970517
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2325340	A		72	H01L-023/36	
DE 19821715	A1			H01L-023/50	
CN 1199927	A			H01L-023/50	
JP 11045956	A		16	H01L-023/12	
KR 98083733	A			H01L-023/12	
KR 98083734	A			H01L-023/12	
US 6060778	A			H01L-023/10	
KR 220249	B1			H01L-023/12	

Abstract (Basic): GB 2325340 A

An integrated circuit **package** comprises an interconnection substrate (50) with a conductive trace layer on each side. A first side (50b) is bonded to a thermally conductive layer (35). The substrate and thermally conductive layer are essentially square, with a hole (36) in the centre. An integrated circuit device (40) is located in the central hole and connected to bond pads on the conductive traces on the second side of the insulating substrate before being **encapsulated** (42) and fixed in the hole. **Solder balls** connect to the conductive traces on the second side of the insulating layer. Preferably the first side of the insulating layer has an epoxy or polyimide layer around its periphery. The thermally conductive layer is made from aluminium silver or copper.

USE - The **ball grid** array **package** is used for integrated circuit devices used in portable equipment such as mobile telephones, pocket computers etc.

ADVANTAGE - The device **package** is low-profile, light, cheap

to make and has excellent heat dissipation properties.
Dwg.3/15

21/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012095682
WPI Acc No: 1998-512593/199844
XRPX Acc No: N98-400303
Mounting method of **BGA package** for PCB, semiconductor IC - involves forming several through holes on **BGA package**, through which reflow solder **heat** is **circulated** between **BGA package** and PCB
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10223798	A	19980821	JP 9727389	A	19970212	199844	B

Priority Applications (No Type Date): JP 9727389 A 19970212
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10223798	A		6	H01L-023/12	

Abstract (Basic): JP 10223798 A
The method involves forming several through holes (8) on a **BGA package**. Several **solder balls** (7) are arranged in matrix shape on the back side of the **BGA package**.
The **BGA package** includes a bare chip which is resin sealed. Reflow solder heat between **BGA package** and a PCB (10), is circulated along the through hole to equalise the temperature between them.
ADVANTAGE - Enables reliable solder joining.
Dwg.1/12

21/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012049885
WPI Acc No: 1998-466795/199840
XRPX Acc No: N98-363626
Ball grid array integrated circuit **package** with EMI shielding - includes **heat spreader** which is electrically connected to **solder balls** via plated through holes extending through dielectric body
Patent Assignee: NORTHERN TELECOM LTD (NELE)
Inventor: MARCANTONIO G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5796170	A	19980818	US 96601667	A	19960215	199840	B

Priority Applications (No Type Date): US 96601667 A 19960215
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
US 5796170 A 9 H01L-023/48

Abstract (Basic): US 5796170 A

The **package** (200) includes a **heat spreader** (214) on one side of a dielectric body (224,226,228) comprising a layer of thermally and electrically conductive material. The body surrounds a die attach area on the **heat spreader** and provides a number of bond pads (216). Interconnections (218) extend from the pads via plated holes extending through the body to a number of **solder balls** (230) of a **ball grid** array on the other side of the body.

A conductive interconnection is provided between the **heat spreader** and selected **solder balls** (231) to provide a ground connection. The ground connection is provided by external rows of **solder balls** extending around sides of the **package** or by clusters of **solder balls** surrounding **balls** for carrying signals.

USE - For use in e.g. telecommunications.

ADVANTAGE - Has improved shielding of electromagnetic interference since the **heat spreader** functions also as a Faraday shield.

Dwg.4/8

21/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011786691
WPI Acc No: 1998-203601/199818
XRAM Acc No: C98-064305
XRPX Acc No: N98-162311
BGA package structure - has resin coating that covers back side of substrate at position corresponding to heat dissipation pores
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10056097	A	19980224	JP 96212373	A	19960812	199818	B

Priority Applications (No Type Date): JP 96212373 A 19960812
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 10056097 A 6 H01L-023/12

Abstract (Basic): JP 10056097 A

The structure has a substrate (2) on which a semiconductor chip (1) is mounted. Multiple heat dissipation pores (7) are formed in the substrate. A conductive wiring (6) of the substrate is electrically connected with the semiconductor chip. Multiple **solder balls** (9) are arranged in the shape of lattice on the back side of the substrate.

The **solder balls** are electrically connected with the conductive wirings. The substrate surface is sealed by a sealing resin (5). The back side of the substrate corresponding to the **heat** dissipation pores, are **covered** by a resin coating (8).

ADVANTAGE - Prevents moisture through heat dissipation pores. Reduces moisture absorption of semiconductor device. Prevents crack generation during mounting.

Dwg.1/5

21/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011676272
WPI Acc No: 1998-093181/199809
XRPX Acc No: N98-074413
Ball grid array **package** type semiconductor device - has **cover** plate which conducts **heat** emitted from chip and is partially bonded to stiffener which is used to maintain flat property of TAB tape with **solder ball**
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9321085	A	19971212	JP 96136287	A	19960530	199809	B

Priority Applications (No Type Date): JP 96136287 A 19960530
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9321085	A		13	H01L-021/60	

Abstract (Basic): JP 9321085 A

The semiconductor device includes a TAB tape (1) which has a **solder ball** (9). A semiconductor IC chip (5) which uses the **solder ball** as the exterminal, is bonded to the TAB tape. A stiffener (2) is bonded to maintain the flat property of the TAB tape.

A cover plate (7) is provided to conduct heat emitted from the chip. The cover plate is partially bonded to the stiffener.

ADVANTAGE - Controls generation of crack resulting from heat on **solder ball**.

Dwg.1/11

21/3,AB/17 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07062267
FAILURE ANALYZING METHOD OF SEMICONDUCTOR DEVICE

PUB. NO.: 2001-289905 [JP 2001289905 A]
PUBLISHED: October 19, 2001 (20011019)
INVENTOR(s): OZAWA TADASHI
APPLICANT(s): NEC CORP
APPL. NO.: 2000-104457 [JP 2000104457]
FILED: April 06, 2000 (20000406)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a failure analyzing method of semiconductor device capable of physically and electrically analyzing a failure.

SOLUTION: In analyzing the failure of a semiconductor device having a silicon substrate as a semiconductor chip for arranging a **heat radiating heat spreader** on the reverse and arranging a

solder ball for **BGA** on a surface and a ceramic substrate for arranging a micro **solder ball** on one surface and arranging the silicon substrate on the other surface, the **solder ball** for the **BGA** and the ceramic substrate are removed (S105), and then, the micro **solder ball** is removed to expose a pad of the silicon substrate (S107). The reverse of the silicon substrate is mounted on an analyzing **package** (S108), and after performing a required wire bonding wire, the analysis to the silicon substrate is carried out (S109).

21/3,AB/18 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

07039823
TAPE **BGA** SEMICONDUCTOR **PACKAGE**

PUB. NO.: 2001-267457 [JP 2001267457 A]
PUBLISHED: September 28, 2001 (20010928)
INVENTOR(s): OTAKA TATSUYA
YOSHIOKA OSAMU
MURAKAMI HAJIME
SUGIMOTO HIROSHI
SUZUKI YUKIO
OMORI TOMOO
APPLICANT(s): HITACHI CABLE LTD
APPL. NO.: 2000-078839 [JP 200078839]
FILED: March 21, 2000 (20000321)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a tape **BGA** semiconductor **package** which is excellent in mass productivity and electric reliability.

SOLUTION: In the tape **BGA** semiconductor **package** , a semiconductor element 6 is mounted on a first region on a metallic plate 15 as a reinforcing and **heat-radiating** plate, a TAB tape 20 having a predetermined wiring pattern 2 is bonded on a second region on the metallic plate 15, the semiconductor element 6 and the wiring pattern 2 are connected by bonding wires 4, and a **solder ball** 1 is positioned on the side of the tape 20 opposed to the plate 15. An opening 9 to the plate 15 is made in the tape 20, a plated layer 11 having an exposed surface facing the opening 9 is provided on the plate 15, and a grounding wire of the wiring pattern 2 of the tape 20 is electrically connected with the plated layer 11 at the exposed surface of the plate 15 by means of a conductive member (the solder 9 or bonding wire 4) provided in the opening 9.

21/3,AB/19 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06708854
BALL GRID ARRAY **PACKAGE** WHERE STRESS IS ALLEVIATED

PUB. NO.: 2000-294686 [JP 2000294686 A]
PUBLISHED: October 20, 2000 (20001020)
INVENTOR(s): JOHNSON ERIC A
KRESGE JOHN S
APPLICANT(s): INTERNATL BUSINESS MACH CORP (IBM)
APPL. NO.: 2000-065422 [JP 200065422]
FILED: March 09, 2000 (20000309)
PRIORITY: 272517 [US 99272517], US (United States of America), March 19, 1999 (19990319)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce strain induced by the heat of the **solder ball** of a **ball grid** array module attached to a circuit card by a vacant part substantially surrounding the second section of a dielectric layer, and a pad **containing** the step positioned above the second section.

SOLUTION: A **solder ball** 48 is attached to a circuit card bad 54, and a **BGA** module 40 is connected to a circuit card 50. A circular vacant space 43 of height ΔH1 inside a board 42 surrounds board material under the GBA pad 44, and a circular vacant space 56 of height ΔH2 inside a board 52 surrounds board material under a circuit card pad 54. The transformation of **heat**-induced strain is **dispersed** to the height H+ΔH1+ΔH2, whereby the strain of the **solder ball** decreases. This protects the preservability of solder connection, and extends the fatigue life of the **BGA** module, and further it can be used together with other method with a slight additional cost.

21/3,AB/20 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

06491992
THERMALLY AND ELECTRICALLY REINFORCED SEMICONDUCTOR **PACKAGE**

PUB. NO.: 2000-077575 [JP 2000077575 A]
PUBLISHED: March 14, 2000 (20000314)
INVENTOR(s): WANG SHINSEN
LEE DONGSHEN
CHEN POFAN
APPLICANT(s): IND TECHNOL RES INST
APPL. NO.: 10-243945 [JP 98243945]
FILED: August 28, 1998 (19980828)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **package** which offers satisfactory **heat radiating** efficiency and reinforced EM shielding.

SOLUTION: This **package contains** a board 20, and a semiconductor chip or die 22 is bonded to the board 20 by a die attaching material, for example, die-adhering epoxy 24. The die 22 and the board 20 are connected with each other by a signal transmitting means, for example, bonding wires 26. A **ball grid** array(**BGA**), preferably **solder** bumps (**balls**) 28 are formed on the underside of the board 20. The solder

bumps 28 are used for external, electrical connection to the chip, and the ends of the conductive traces in the board are connected with the solder bumps 28. A **heat radiating** body 32, provided with a supporting portion connected to a ground pad 34, is placed on the die 22, and the gaps between the board 20, the die 22 and the **heat radiating** body 32 are filled with a molded compound 30.

21/3,AB/21 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

06491980
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2000-077563 [JP 2000077563 A]
PUBLISHED: March 14, 2000 (20000314)
INVENTOR(s): SUMINOE SHINJI
ISOBE YASUAKI
TOYOSAWA KENJI
APPLICANT(s): SHARP CORP
APPL. NO.: 10-246215 [JP 98246215]
FILED: August 31, 1998 (19980831)

ABSTRACT

PROBLEM TO BE SOLVED: To effectively dissipate heat produced during the manufacture of the **package** of a **BGA** semiconductor device, and prevent **package** failures caused by heat and stresses produced during manufacture for reduction in the size and thickness of the **package** and its pitch and increase in a number of terminals.

SOLUTION: Inner leads 1a and outer leads 1b are formed only on an insulating tape 2. A semiconductor chip 3 is jointed with the inner leads 1a via anisotropic conductive material 5 by flip-chip bonding. A **heat** sink 7, **covering** at least the entire region where **solder balls** 9 connected with the outer leads 1b are to be formed, is jointed with the insulating tape 2 via an adhesive. Unlike TAB method, the inner leads 1a are not exposed on the insulating tape 2 and are prevented from being deformed as much as possible.

21/3,AB/22 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

06436453
BGA PACKAGE AND MANUFACTURE THEREOF

PUB. NO.: 2000-022020 [JP 2000022020 A]
PUBLISHED: January 21, 2000 (20000121)
INVENTOR(s): TANAKA HIROBUMI
TANAKA JUNSUKE
FUJITA KAZUTO
SHIODA TAKASHI
MORITA MORIJI

APPLICANT(s): MITSUI CHEMICALS INC
APPL. NO.: 10-182669 [JP 98182669]
FILED: June 29, 1998 (19980629)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **BGA** with terminal especially increasing the fitting intensity of a hand ball and the manufacturing method thereof.

SOLUTION: In a **BGA package** with terminal and manufacturing method thereof, for the purpose of fitting a **solder ball** 1 to a ball pad 8 annexed to a terminal part 2 of the **BGA package** with terminal, the **solder ball** 1 is fed with sufficient heat by combined use of the heating adopting the infrared ray irradiation and the **circulated** nitrogen **hot** wind so as to increase the fitting intensity of the **solder ball** 1.

21/3,AB/23 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

06221624
SEMICONDUCTOR DEVICE

PUB. NO.: 11-163186 [JP 11163186 A]
PUBLISHED: June 18, 1999 (19990618)
INVENTOR(s): TAKANO EIJI
HOSOMI HIDEKAZU
TAKUBO TOMOAKI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 09-330210 [JP 97330210]
FILED: December 01, 1997 (19971201)

ABSTRACT

PROBLEM TO BE SOLVED: To enable a **BGA package** provided with a cover plate to be warped less, even when a resin board is used.

SOLUTION: A **BGA package** 11 is constituted of a resin **BGA** board 12 and a cover plate 16. A large number of **solder ball** terminals 13 are provided to the underside of the **BGA** board 12, and a chip connecting electrode is formed on the upside of the **BGA** board 12. A semiconductor chip 14 is connected to the electrode in a flip-chip mounting manner. The cover plate 16 is bonded to the **BGA** board 12 with an adhesive agent 17 for covering the semiconductor chip 14, and formed through in such a way that a copper plate is bent into the cover plate 16 of an integral structure composed of a top plate 16a and sides 16c connected to the top plate 16a with joints 16b. The **cover** plate 16 is **heated** when it is bonded to the board 12, and a cutout is provided to each of the four corners of the cover plate 16, so that stresses imposed on the **BGA** board 12 can be relaxed, and the board 12 is reduced less.

21/3,AB/24 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

06113123
MANUFACTURE OF SOLDER BUMP ELECTRODE AND SOLDER BUMP ELECTRODE

PUB. NO.: 11-054656 [JP 11054656 A]
PUBLISHED: February 26, 1999 (19990226)
INVENTOR(s): ITO KATSUMI
APPLICANT(s): NEC CORP
APPL. NO.: 09-220972 [JP 97220972]
FILED: July 31, 1997 (19970731)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method of manufacturing solder bump electrodes that can maintain a predetermined interval between a substrate and a **package** and permit stable mounting, even if there are variations in mounting temperature by providing a structure, in which a high melting-point **solder ball** or conductive metal ball is **covered** with a low **melting**-point **solder ball** and by making the size of the high melting-point **solder ball** or conductive metal ball equal to a desired predetermined interval, in a **BGA package**.

SOLUTION: An opening is formed only at a terminal portion 2 in a solder resist 1 which is applied over the entire surface of a **package** substrate 3. A small quantity of liquid high melting point solder 4 is dropped. Such a small quantity of solder 4 becomes spherical by the surface tension and solidifies. An appropriate quantity of liquid low melting point solder 6 is dropped, so that a low melting point **solder ball** 7 is formed so as to **cover** the high **melting** point **solder ball** 5 formed as described.

21/3,AB/25 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

06085144
PACKAGE STRUCTURE OF **BGA** SEMICONDUCTOR DEVICE

PUB. NO.: 11-026658 [JP 11026658 A]
PUBLISHED: January 29, 1999 (19990129)
INVENTOR(s): KAKU YOSHITAKA
APPLICANT(s): ROHM CO LTD
APPL. NO.: 09-184203 [JP 97184203]
FILED: July 09, 1997 (19970709)

ABSTRACT

PROBLEM TO BE SOLVED: To improve the radiation efficiency of a **package** to avoid damaging a semiconductor due to the heat staying therein by roughening the surface of the **package** for the **heat radiation**.

SOLUTION: The **BGA** semiconductor device has a chip 2 fixed to a substrate 1 and **solder balls** 5 on the substrate surface are made conductive to the chip through inner leads 4 by the wire bonding 3. On the substrate, a resin-molded **package** P is formed and has a rough surface M to increase the radiation area. Such rough surface M increases

the **package** surface area enough to well **radiate** the **heat** staying in the **package** P. A Cu heat sink is adhered to the inner bottom of a recess to more improve the **radiation** efficiency. The **heat** sink may be contacted to the chip 2 on the substrate 1 to much **radiate** the **heat** staying in the chip 2.

21/3,AB/26 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

05978574
SEMICONDUCTOR DEVICE AND FABRICATION THEREFOR

PUB. NO.: 10-261674 [JP 10261674 A]
PUBLISHED: September 29, 1998 (19980929)
INVENTOR(s): HATAKEYAMA MAKOTO
OKANE NOBORU
SATO TAKAO
ONO JUNICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-223672 [JP 97223672]
FILED: August 20, 1997 (19970820)

ABSTRACT

PROBLEM TO BE SOLVED: To facilitate handling, while enhancing productivity by handling at least one of a **package** board, a first holder or a second holder as a long body arranged with a plurality of chip-mounting regions, and the like, at constant intervals in the longitudinal direction.

SOLUTION: A long stiffener is bonded with a TAB tape piece of good quality by an adhesive. The element-forming face of a chip is covered with an epoxy resin, for example, under a state connected with the TAB tape and is **thermally** set. A **cover** plate piece is bonded onto the long stiffener and to the rear side of the chip by an adhesive. Subsequently, a conductor pad is formed at a ball, connecting position around the chip mounting region on the rear side of the TAB tape, affixed with the stiffener and coated with flux before being bonded with a eutectic **solder ball**. Furthermore, it is heated to activate the flux and to connect the eutectic **solder ball** with a pad. Finally, it is cut off to obtain a **BGA package**.

21/3,AB/27 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

05964603
BALL GRID ARRAY **PACKAGE** AND PRINTED BOARD

PUB. NO.: 10-247703 [JP 10247703 A]
PUBLISHED: September 14, 1998 (19980914)
INVENTOR(s): FUKUNAGA NORIKAZU
APPLICANT(s): SUMITOMO KINZOKU ELECTRO DEVICE KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-069159 [JP 9769159]

FILED: March 05, 1997 (19970305)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a **ball grid** array **package** and a printed board excellent in **heat radiation**.

SOLUTION: When this array **package** 10 comprises a mounting part of a semiconductor element 11 and a **solder ball** 12 under a **heat radiation** part on the upper face, a **heat radiation** block 21 excellent in heat conductivity is provided near under the semiconductor element 11. A wing part extending further laterally beyond the semiconductor element 11 may be provided. It is preferable that a gap between the upper face of the **heat radiation** block 21 and the lower face of the semiconductor element 11 is electrically insulated via a high heat conductive resin or a high heat conductive resin sheet. It is preferable that high heat conductive adhesives or grease is filled between the array **package** 10 and printed wiring board 41.

21/3,AB/28 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

05964602
BALL GRID ARRAY **PACKAGE** AND PRINTED BOARD

PUB. NO.: 10-247702 [JP 10247702 A]
PUBLISHED: September 14, 1998 (19980914)
INVENTOR(s): FUKUNAGA NORIKAZU
APPLICANT(s): SUMITOMO KINZOKU ELECTRO DEVICE KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-069157 [JP 9769157]
FILED: March 05, 1997 (19970305)

ABSTRACT

PROBLEM TO BE SOLVED: To improve the **heat radiating** property, by a method wherein a **heat radiating** board in excellent **thermal** conductivity is junctioned with the bottom face side of the semiconductor element mounting part of a resin substrate having the semiconductor element mounting part on the top face side, with the junctioning **pad** of a **solder ball** on the bottom face side.

SOLUTION: A **ball grid** array **package** 10 is provided with a resin substrate 13 having the mounting part of a semiconductor element 11 on the top face side thereof while having a **solder ball** junctioning **pad** on the bottom face side thereof. On the other hand, a **heat radiating** board 21 in excellent thermal conductivity is junctioned with the bottom face side of the semiconductor element mounting part of the resin substrate 13. Resultantly, the heat dissipated from the bottom face of the semiconductor element 1 is radiated to a printed substrate 41 in almost the shortest distant path. Besides, the **heat radiating** board 21 formed of a material in excellent thermal conductivity such as copper, etc., also takes a planar shape at the lower thermal resistance, thereby enabling the semiconductor element 11 to efficiently **radiate** the **heat** to the printed wiring board 41.

21/3,AB/29 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

05767777
SEMICONDUCTOR **PACKAGE**

PUB. NO.: 10-050877 [JP 10050877 A]
PUBLISHED: February 20, 1998 (19980220)
INVENTOR(s): OGAWA HIDENORI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-200287 [JP 96200287]
FILED: July 30, 1996 (19960730)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor **package** in which reliability of mechanical and electrical connection can be improved by **dispersing** and absorbing occurring **thermal** stress.

SOLUTION: A **BGA** type semiconductor **package** has a rectangular tape carrier 10. A number of **soldering balls** 16 are provided on the under face of the tape carrier and a semiconductor chip 18 is mounted on the top face. A rectangular stiffener sticks on the top face of the tape carrier so as to surround the semiconductor chip. Further, a rectangular cover plate 30 sticks on the top face of the stiffener and on the top face of the semiconductor chip. A plurality of slits 26 for absorbing and **dispersing thermal** stress occurring owing to changes in temperature are opened in corner parts of the stiffener.

21/3,AB/30 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

05706285
SEMICONDUCTOR DEVICE AND ITS ASSEMBLING METHOD

PUB. NO.: 09-321085 [JP 9321085 A]
PUBLISHED: December 12, 1997 (19971212)
INVENTOR(s): OYA NOBUAKI
OKUTOMO TAKAYUKI
TAGUCHI HIDEO
IKEMIZU MORIHIKO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-136287 [JP 96136287]
FILED: May 30, 1996 (19960530)

ABSTRACT

PROBLEM TO BE SOLVED: To suppress the occurrence of cracks caused by heat, at the **solder ball** of a **BGA package** type semiconductor device which has **heat radiation** member, by partially bonding a **heat radiation** member to a flattening member.
SOLUTION: This semiconductor device is provided with a chip carrier 1 which has a group of ball-shaped electrodes 9, a semiconductor integrated circuit chip 5 which is electrically connected to the chip carrier 1 and in which the group of ball-shaped electrodes 9 serve as external terminals, and a flattening member 2 for keeping the flatness of the chip carrier 1. Furthermore, this is provided with a heat dissipating member 7 for letting

go the heat generated from the semiconductor integrated circuit 5, being thermally coupled with the semiconductor integrated circuit chip 5. Then, the heat dissipating member 7 is bonded partially to the flattening member 2. For example, a stainless fastener is bonded by an adhesive 3 onto the TAB tape 1, and thereon a copper cover plate 7 is bonded partially only at a projection 12 for bonding by an adhesive 8

21/3,AB/31 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO

05645754
SEMICONDUCTOR **PACKAGE**

PUB. NO.: 09-260554 [JP 9260554 A]
PUBLISHED: October 03, 1997 (19971003)
INVENTOR(s): ASAI HIRONORI
YANO KEIICHI
IYOGI YASUSHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-072271 [JP 9672271]
FILED: March 27, 1996 (19960327)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **BGA**(**ball grid** array) **package** which does not need a **heat radiation** fin even in **case** that a high-output semiconductor element is mounted, and besides in which the reliability of connection between a **package** and a mounting board is improved.

SOLUTION: The heat of an element is let go and **radiated** from a **heat** conductive to a mounting board without needing a **heat radiation** fin by joining the heat conductive plate 20 consisting of material high in heat conductivity to the bottom of a **package** substrate 10 provided with an opening 12, and joining a semiconductor element 30 to the topside, and joining the bottom of the heat conductive plate to a mounting board 60. Moreover, the heat conductive plate and the mounting board are fixed with each other by a projection and a recess 61, 21 provided respectively. Hereby, the stress accompanying the thermal expansion coefficient decreases, and the breakage of a **solder ball** connection is eliminated.

? T S26/3,AB/1-4

26/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013911990
WPI Acc No: 2001-396203/200142
Related WPI Acc No: 2001-281122
XRPX Acc No: N01-291805
Integrated circuit **package** mounted on printed **circuit board** has eutectic solder mass in lower surface of **package** substrate, in areas where **solder ball** mounted on base substrate has highest joint strain energy density
Patent Assignee: NORTEL NETWORKS LTD (NELE)
Inventor: KATCHMAR R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6194782	B1	20010227	US 98103802	A	19980624	200142	B

Priority Applications (No Type Date): US 98103802 A 19980624
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6194782	B1		14	H01L-023/34	

Abstract (Basic): US 6194782 B1
Abstract (Basic):

NOVELTY - An eutectic solder mass (26) is located on the lower surface of the **package** substrate (12), in the areas where the **solder balls** mounted on base substrate (28) has highest joint strain energy density. The solder mass adheres the **package** substrate and the base substrate.

DETAILED DESCRIPTION - The **package** substrate (12) has interconnected conductive traces on upper and lower surfaces. A semiconductor die (18) mounted either on or adjacent to the upper surface of the **package** substrate, is connected with the conductive traces in the upper surface. An array of **solder balls** (24) which are mounted on the lower surface of the substrate, are connected with the conductive traces in the lower surface. The highest joint strain energy density WGi is calculated by the equation
WGi=ki(DNPi(approximatelyas-approximatelyapkg)iapproximatelyDTi)2,
ki=1divide4ni summation of (1divideDELTAKj)j-1,i,
DELTAKj=(PdivideDELTADNP)jdivide(1divideEh)t+1divide(Eh)pkg)j, where alphas is the local coefficient of thermal expansion of substrate, alphapkg is logical coefficient of thermal expansion of the **package** substrate. DNPi is distance between **solder ball** and the neutral point of **package**, i' is i-th **ring** of joints from the neutral point of **package**, ni is the number of terminations of the **solder ball**, P is joint pitch within the **solder ball**, E' is modulus of elasticity, h' is structural thickness, t' termination which forms a joint when mounted pkg is the **package**, DELTADNP is the change in the distance from the neutral point of the **package** between successive balls and DELTATi is the temperature excursion through which the i-th ball cycles.

USE - In e.g. plastic **ball grid** array **package**,

surface mounted area array **package**, chip scale **package**, ceramic column grid array **package** mounted on printed **circuit board** (PCB).

26/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013750590
WPI Acc No: 2001-234819/200124
XRAM Acc No: C01-070276
XRPX Acc No: N01-167934
Semiconductor device **package**, e.g. **ball grid** array type **package**, uses pieces of adhesive film to attach a semiconductor die to an **interposer** having interconnects
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: JIANG T
Number of Countries: 090 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200109939	A1	20010208	WO 2000US20583	A	20000728	200124	B
AU 200063879	A	20010219	AU 200063879	A	20000728	200129	

Abstract (Basic): WO 200109939 A1
Abstract (Basic):
NOVELTY - A semiconductor device **package** consists of a semiconductor die; an electrically conductive external terminal; an **interposer**; and pieces of adhesive film disposed between the semiconductor die and the **interposer** to adhere the semiconductor die to the die-attach surface of the **interposer**.
DETAILED DESCRIPTION - A semiconductor device **package** comprises a semiconductor die (12); an electrically conductive external terminal; an **interposer** (16); and pieces of adhesive film. The semiconductor die has a first surface where an integrated circuit and an electrically conductive bond pad (14) are fabricated. The **interposer** has a die-attach surface, an external surface opposite the die-attach surface, and an electrically conductive interconnect (18) electrically coupling the bond pad to the external terminal. It is disposed between the semiconductor die and the external terminal. The pieces of adhesive film are disposed between the semiconductor die and the **interposer** to adhere the semiconductor die to the die-attach surface of the **interposer**. An INDEPENDENT CLAIM is also included for a method of **packaging** a semiconductor device by laminating pieces of adhesive film to an **interposer**, attaching the semiconductor die to the **interposer**, and bonding the electrically conductive interconnect to the electrically conductive bond pad.
USE - As semiconductor device **package**, e.g. **ball grid** array type **package**.

26/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013653201
WPI Acc No: 2001-137413/200114
XRAM Acc No: C01-040269
XRPX Acc No: N01-100092
Ball grid package for a silicon chip comprises conductive leads configured to prevent interference of external

electromagnetic fields
Patent Assignee: SILICONWARE PRECISION IND CO LTD (SILI-N)
Inventor: LIN S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6184580	B1	20010206	US 99394263	A	19990910	200114	B

Priority Applications (No Type Date): US 99394263 A 19990910
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6184580	B1		7	H01L-023/34	

Abstract (Basic): US 6184580 B1
Abstract (Basic):

NOVELTY - A **ball grid** array **package** comprises conductive leads and a substrate that are positioned below a **heat sink**. A silicon chip is connected to contact points on a surface of the substrate and the conductive leads by bonding wires. **Solder balls** are attached to some of the contact points. The bonding wires, portion of the conductive leads, and the silicon chip are **enclosed** by a molding compound.

DETAILED DESCRIPTION - A **ball grid** array **package** comprises a first **heat sink** (26) having an exposed surface (47), a bottom surface, and a die-attach region (24) on the bottom surface of the first **heat sink**. Each of conductive leads (36) is divided into an inner lead portion and an outer lead portion. The inner lead portions are in contact with the bottom surface of the first **heat sink** and surrounds the die-attach region, and the outer lead portions extend away from the bottom surface of the first **heat sink**. A substrate (35) has a first surface (31) and a second surface (33), in which the first surface is in contact with the conductive leads so that the inner lead portions are sandwiched between the first **heat sink** and the substrate, and the second surface has contact points (49, 50, 64, 66). A silicon chip (20) is attached on the die-attach region on the bottom surface of the first **heat sink**. It has an active surface (21) and a back surface (22), and the back surface is in contact with the bottom surf ace of the first **heat sink**. Bonding wires (25, 27) electrically connect the inner lead portion and some of the contact points on the second surface of the substrate to the active surface of the silicon chip. **Solder balls** (29) are mounted on some of the contact points on the second surface of the substrate. The outer lead portions are further used to support the ball array **package** when attached to a **circuit board** (60). A molding compound (28) **encloses** the bonding wires, the silicon chip, the inner lead portion of the conductive leads, and the contact points electrically connected to the silicon chip.

26/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013359647
WPI Acc No: 2000-531586/200048
XRPX Acc No: N00-393003
Electronic **packaging** assembly has socketing substrate coupled to **motherboard** and embedded with array of electrically conductive pins

attached to **solder balls**
Patent Assignee: INTEL CORP (ITLC)
Inventor: KABADI A N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6097609	A	20000801	US 98223647	A	19981230	200048	B

Priority Applications (No Type Date): US 98223647 A 19981230
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6097609	A		7	H05K-007/02	

Abstract (Basic): US 6097609 A
Abstract (Basic):
NOVELTY - The bottom surface of a socketing substrate (335), is aligned horizontally with a **motherboard** (300). An array of electrically conductive pins (340) are embedded through the socketing substrate. The pins have top and bottom ends facing the **motherboard**. The socketing substrate is coupled to the **motherboard** through a series of **solder balls** (345) which are attached to the bottom of the pins.
DETAILED DESCRIPTION - An electronic component (320) is electrically coupled to the array of pins on the socketing substrate via array of lands (325) on the bottom side of the component. A lid (350) covers the electronic component and wraps around the vertical sides of the socketing substrate.
USE - E.g. **BGA** and LGA **package**.
ADVANTAGE - Provides a novel design for mounting a **BGA** or LGA component onto board without using a **stiffener**, gold plating or a separate **interposer** and socketing stage, hence cost is reduced considerably.
DESCRIPTION OF DRAWING(S) - The figure shows the side view of the assembly applied to a dual sided **motherboard** mounted with electronic components.

26/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013010161
WPI Acc No: 2000-182013/200016
XRPX Acc No: N00-134363
Solder ball attaching method for connecting integrated circuit **package** and **circuit boards**
Patent Assignee: ADVANCED INTERCONNECTIONS (ADIN-N); ADVANCED INTERCOMMUNICATIONS CORP (ADIN-N)
Inventor: MURPHY J V
Number of Countries: 021 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9966599	A1	19991223	WO 99US13038	A	19990611	200016	B
US 6007348	A	19991228	US 96646109	A	19960507	200016	
			US 96694740	A	19960809		
			US 9894957	A	19980615		
EP 1088371	A1	20010404	EP 99927403	A	19990611	200120	
			WO 99US13038	A	19990611		

Abstract (Basic): WO 9966599 A1
Abstract (Basic):
NOVELTY - A graphite made assembly fixture has rounded cavities located in pattern corresponding to pattern of holes (64) in the insulative support (62). Each cavity is filled with **solder ball** (52). The support is positioned over the assembly fixture so that bottom end (54) of the socket terminals (50) contacts the corresponding **solder ball**. The **solder ball** is **soldered** to the bottom end of the socket terminal.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for intercoupling component of type used to couple an array of electrical connection regions disposed on one substrate to array of electrical connection regions disposed on another substrate.
USE - For connecting IC **package** such as **BGA package** and **circuit boards**.
ADVANTAGE - Positioning **ring** along axial length of socket terminal minimizes bending or warping of support due to forces imparted by socket terminals when press-fit within the support.

26/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012913838
WPI Acc No: 2000-085674/200007
XRAM Acc No: C00-023903
XRPX Acc No: N00-067168
Thermally enhanced tape **ball grid** array **package**
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: CHIA C J; LIM S; LOW O H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6002169	A	19991214	US 9897883	A	19980615	200007	B

Abstract (Basic): US 6002169 A
Abstract (Basic):
NOVELTY - Holes are arranged in an array pattern through a tape substrate to expose conductive metal traces on the substrate top. A nonconductive **stiffener** frame is attached to the substrate bottom and has through holes corresponding to those in the substrate. An IC mounted on the substrate is electrically connected to the traces. **Solder balls** are attached to the exposed traces to allow electrical connection of the **package** to a printed **circuit board** (PCB).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **stiffener** frame for use in the **package**, comprising aluminum that has been anodized to form a protective insulating coating. The **stiffener** frame dissipates heat produced by the IC.
USE - The anodized aluminum frame serves the dual purpose of supporting the tape automated bonding (TAB) substrate during assembly and dissipating heat generated by the IC chip **package**.
ADVANTAGE - Improved thermal performance, and thus improved device reliability.

26/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012867068
WPI Acc No: 2000-038901/200003
XRAM Acc No: C00-010028
XRPX Acc No: N00-029330
Packaging component for integrated circuit die used in printed **circuit boards**
Patent Assignee: MINNESOTA MINING & MFG CO (MINN); 3M INNOVATIVE PROPERTIES CO (MINN)
Inventor: HARVEY P M; PLEPYS A R
Number of Countries: 024 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9957764	A1	19991111	WO 99US7087	A	19990331	200003	B
US 6140707	A	20001031	US 9874126	A	19980507	200057	
EP 1082762	A1	20010314	EP 99914308	A	19990331	200116	
			WO 99US7087	A	19990331		

Abstract (Basic): WO 9957764 A1
Abstract (Basic):
NOVELTY - The **packaging** component comprises flexible dielectric tape (60) whose upper surface has selected pattern of conductive traces (62) made of die attachment pads (56) and **ball-grid**-array (**BGA**) attachment pads (64) and lower surface has openings for exposing **BGA** attachment pads. Conductive traces are covered by dielectric adhesive layer (58) attached with **stiffener** (52) having a window.
DETAILED DESCRIPTION - Openings in the adhesive expose die attachment pads.
INDEPENDENT CLAIMS are included for the following: (i) A **packaged** integrated circuit which has **packaging** component **containing BGA solder balls** (30) attached to **BGA** attachment pads through the opening and an integrated circuit die (32) disposed within the window formed in the **stiffener**. (ii) Manufacture of **packaging** component. The **stiffener** is

laminated on dielectric adhesive layer using an adhesive. A window is formed in the **stiffener** by etching to expose a portion of the tape and adhesive overlying the die attachment pads. The adhesive overlying die attachment pads are then removed.

USE - The **packaging** component is used for flip-chip integrated circuit die used in printed **circuit boards**.

26/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012804034
WPI Acc No: 1999-610264/199952
XRPX Acc No: N99-449616
Ball grid array (**BGA**) **package** fabrication method for **circuit board** of computer system
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: CARICHNER K Y; LIANG D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5972734	A	19991026	US 97932711	A	19970917	199952	B

Abstract (Basic): US 5972734 A
Abstract (Basic):

NOVELTY - A die (206) is bonded in a cavity (204) of a substrate (202) on whose surface conductive traces (212) are formed. **Interposers** (220) each having a hole, are positioned on the traces. The holes of the **interposers** are filled with a conductive material (208) which connects to the traces. **Solder balls** (214) are formed on the **interposers** and are connected to the traces through the conductive material.

USE - For fabricating a **BGA package** for mounting on **circuit boards** used in computer systems and electronic appliances such as television sets, microwave ovens, automobiles, aircraft, digital wrist watches, etc.

ADVANTAGE - Allows simple trace paths, while retaining coplanarity of the **solder balls**. Provides greater **encapsulation** height.

26/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012698393
WPI Acc No: 1999-504502/199942
XRPX Acc No: N99-377310
Potential measurement **circuit** for **circuit board** in PGA **package**, IC **package** - has several through-holes configured from cover plate to current carrying section of **circuit board** through **stiffener**
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11220057	A	19990810	JP 9819673	A	19980130	199942	B

Abstract (Basic): JP 11220057 A

NOVELTY - Semiconductor chip (16) is mounted in rear side of **solder ball** (15). A **stiffener** (19) is used to fix **circuit board**. A cover plate (21) is bonded on surface of both chip and **stiffener**, using an adhesive agent (20). Resin sealing (17) is provided for chip. Several through-holes (22,23) are provided to the current-carrying sections of **circuit board** through **stiffener** from cover plate. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the temperature measurement method of semiconductor chip in PGA **package**.

USE - For measuring potential of arbitrary points on **circuit board** connected to semiconductor chip in PGA **package**, IC chip.

26/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012661768
WPI Acc No: 1999-467873/199939
XRPX Acc No: N99-349296
Test apparatus for semiconductor device **packaged** in surface mount module
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: PATEL J G; THYGESEN D J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5929646	A	19990727	US 96766234	A	19961213	199939	B

Abstract (Basic): US 5929646 A
Abstract (Basic):
NOVELTY - Landing pads (213,214) provide interconnection with a module test card (100) and a **system board** (300) through a top and bottom array of **solder balls** (207,208), respectively. The test card is placed on top of an **interposer** (204) such that top array of landing pads (213) aligns with the **interposer** landing pads (110) and is connected to **interposer** through the top array of **solder balls** (207).
DETAILED DESCRIPTION - The module test card comprises an array of **interposer** landing pads (110) on the underside of a substrate (102) that are connected to the array of module landing pads (104) and test pins (106). A connecting module (202) is placed directly on the landing pads (302) of the **system board** to connect the module (202) to the **system board**.
An INDEPENDENT CLAIM is also included for semiconductor device testing method.
USE - For testing semiconductor device **packaged** in surface mount module such as **ball grid** array module and cylinder grid array module during fabrication of IC.

26/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012422443
WPI Acc No: 1999-228551/199919
Related WPI Acc No: 1998-446271
XRPX Acc No: N99-169095
Ball grid array (**BGA**) **package** is simply removed from printed **circuit board** or **motherboard**
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: KIRKLAND J; SCHNEIDER M R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5885848	A	19990323	US 96724076	A	19960930	199919	B
			US 97901489	A	19970728		

Abstract (Basic): US 5885848 A
Abstract (Basic):
NOVELTY - A lock **ring** (30) with a female threaded opening (38) is positioned on a substrate (14) around a die (18) with the area of the opening greater than the area of the top surface of the die. **Encapsulant** (42) is applied through the opening to cover the die and adhere the lock **ring** to the substrate.
DETAILED DESCRIPTION - A **heat sink** (50) with a male threaded portion (54) can be threaded into the lock **ring**. An INDEPENDENT CLAIM is included for a method of removing the **package** from printed **circuit boards** (PCBs) or **motherboards** for repair or replacement.
USE - None given.
ADVANTAGE - Simplifies removal of the **package** from a PCB or **motherboard** since the **heat sink** can be unthreaded leaving the underlying **package** accessible for solder reflowing.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of the **BGA package**.

26/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012376082
WPI Acc No: 1999-182189/199916
XRAM Acc No: C99-053335
XRPX Acc No: N99-133709
Packaged semiconductor device has a **ball grid** array substrate
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: BABA S
Number of Countries: 004 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19821916	A1	19990311	DE 1021916	A	19980515	199916	B
JP 11074417	A	19990316	JP 97231927	A	19970828	199921	
KR 99023135	A	19990325	KR 9818023	A	19980519	200024	
DE 19861009	A1	20010607	DE 1021916	A	19980515	200132	
			DE 1061009	A	19980515		

Abstract (Basic): DE 19821916 A1
Abstract (Basic):
NOVELTY - In a semiconductor device which has a **ball grid** array (**BGA**) substrate consisting of an intermediate insulating layer sandwiched between upper and lower multilayer insulating layers, the insulating layers consist of an organic material with a thermal expansion coefficient matching that of a **circuit board** on which the device is mounted.
DETAILED DESCRIPTION - A semiconductor device has
(a) a **BGA** substrate as described above;
(b) conductors on the top surface of each insulating layer and within the substrate;
(c) **solder balls** on the outer surface of the lower insulating layer; and
(d) a semiconductor chip which has electrodes for connection to the conductors and which is electrically connected to the **solder balls** by vias provided in each insulating layer.
INDEPENDENT CLAIMS are also included for similar semiconductor

devices, in which
(i) the electrodes are arranged in an annular region on the chip and the voltage supply and the earth are connected respectively to electrodes at the outermost and innermost peripheral rows; or
(ii) the device has a resin sealant for intimately contacting the chip with the **BGA** substrate, an external **heat sink** for dissipating heat produced in the chip and a **ring** which both spaces and connects the **BGA** substrate and the **heat sink**.
Preferred Feature: The linear thermal expansion coefficient of the insulating layer material is 1x10 Power(-5) - 6x10 Power(-5)/ degrees C when that of the **circuit board** is 1x10 Power(-5) - 2 x 10 Power(-5) /degrees C.
USE - As a **packaged BGA** ch

26/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012346688
WPI Acc No: 1999-152795/199913
Related WPI Acc No: 1998-427307
XRAM Acc No: C99-045016
XRPX Acc No: N99-110143
Preventing **encapsulant** applied over wire bonded integrated circuit chip from flowing outward onto other electrical connections - comprises applying **ring** of material to substrate around pads and forming annular well in it to create pair of projecting barrier walls
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: FLETCHER M B; FULLER J W; KNIGHT J A; KOTYLO J A; MORING A F; PASSANTE D M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5869356	A	19990209	US 96657469	A	19960529	199913	B
			US 9842875	A	19980317		

Abstract (Basic): US 5869356 A
NOVELTY - Flow of plastic **encapsulant** (32), applied over integrated circuit (IC) chip (26) wire bonded to series of wire bond pads (14) formed on substrate, is controlled by applying barrier material (38) to the substrate surrounding the pads so that it projects upwards from the surface and forming a well (44) in the material to create pair of walls (40,42) projecting from the surface. DETAILED DESCRIPTION - The barrier material is formed with essentially straight walls extending vertically. It is a photo-imaging material, and the well is formed by photo-imaging, or a solder mask material, the surface of the substrate also being solder mask material. It is applied by screen printing. The lead wires of the IC chip are bonded to the wire bond pads after forming the barrier.
USE - In **encapsulating** an IC chip wire bonded to a dielectric substrate to form a chip carrier structure.
ADVANTAGE - S - The barrier material provides a double barrier, in effect, preventing **encapsulant** from flowing outward and covering circuit connection pads, e.g., **ball grid** array pads, which should not be covered, the **encapsulant** almost certainly being constrained by the well in the unlikely event that it is able to extend over the inner wall. DESCRIPTION OF DRAWING(S) - The drawing shows a

sectional view of a carrier with a chip mounted on a **circuit board** by **solder balls**. (14) wire bond pads; (24) **ball grid** array pads; (26) IC chip; (28) lead wires; (32) **encapsulant**; (38) barrier; (40) inner wall; (42) outer wall; (44) well; (56) **circuit board**.

26/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012228104
WPI Acc No: 1999-034211/199903
XRPX Acc No: N99-025555
Ball grid array **package** - includes multiple wire bonds that connect bonding pads of integrated circuit chip to bonding pads on top surface of substrate and bonding surfaces of conductive **rings**
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: ALAGARATNAM M; CHIA C J; LOW Q H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5841191	A	19981124	US 97837530	A	19970421	199903	B
JP 10326851	A	19981208	JP 98109634	A	19980420	199908	

Abstract (Basic): US 5841191 A

The **package** includes a substrate (10) having a metallic pattern on the surfaces and multiple bonding pads (12) on the top surface. The bonding pads are in contact with the metallic pattern. A pair of raised conductive **rings** (30,32) are mounted on the top surface of the substrate to provide elevated bonding surfaces.

An integrated circuit chip (20) mounted on the top surface of the substrate has a number of bonding pads. Multiple wire bonds (24) interconnect the bonding pads of the chip to the bonding pads on the substrate and to the bonding surface of the conductive **rings**. The bottom contact (14) provided at the bottom surface of the substrate are connected to a **motherboard** through **solder balls**.

ADVANTAGE - Provides conductive **rings** that enable convection of power buses to integrated circuit. Improves power distribution characteristics. Accommodates more bonding pads through multiple tier bonding.

26/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012136296
WPI Acc No: 1998-553208/199847
XRPX Acc No: N98-431963
BGA package mounting structure - has thermal conductive **heat sink** attached to bottom surface of resin substrate
Patent Assignee: SUMITOMO KINZOKU CERAMICS KK (SUMI-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10247702	A	19980914	JP 9769157	A	19970305	199847	B

Priority Applications (No Type Date): JP 9769157 A 19970305
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10247702	A		8	H01L-023/12	

Abstract (Basic): JP 10247702 A
The structure (1) has a **BGA package** (10) mounted on a resin substrate (13). The resin substrate is mounted on a printed **circuit board** (41) through **solder balls** (12).
The **solder balls** are connected to resin substrate through junction pads. A thermal conductive **heat sink** (21) is attached at the bottom surface of resin substrate. Preferably, a heat-dissipating fin (51) is mounted on upper surface of the **BGA package**, to release heat to open air.
ADVANTAGE - Ensures heat dissipation of **BGA package** mounted on printed **circuit board**.
Dwg.1/11

26/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012077995
WPI Acc No: 1998-494906/199842
XRPX Acc No: N98-386527
Circuit board for IC **package** e.g. **BGA package** - has utility region comprising **ring**-like power traces and ground traces formed alternatively, that are connected to respective **solder balls** via through holes with conductive material
Patent Assignee: ACC MICROELECTRONICS CORP (ACCM-N)
Inventor: CHU E; LAI H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5801440	A	19980901	US 95541423	A	19951010	199842	B
TW 347582	A	19981211	TW 95111143	A	19951021	199920	

Abstract (Basic): US 5801440 A
The **circuit board** has a semiconductor die attachment region (12) on one side of an insulated substrate. An utility region

(22) surrounds the die attachment region. The utility region includes **ring**-like ground traces (18) and power traces (24) extended alternately. A single trace region (36) that surrounds the utility region, includes a set of signal traces (40) connected to the semiconductor die via conductors.

Solder balls for connecting to a power source and for earthing are provided on the reverse side of the substrate. A set of through holes with conductive material are formed in the substrate, that connect the ground traces and power traces to respective **solder balls**.

26/3,AB/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011683625
WPI Acc No: 1998-100535/199809
XRAM Acc No: C98-033174
XRPX Acc No: N98-080581
Ball grid array semiconductor **package** has **ring** -type **heat sink** - surrounding the **package** **encapsulation** to effectively dissipate heat and has plated through holes to enhance loss
Patent Assignee: ANAM IND KK (ANAM-N); AMKOR ELECTRONICS INC (AMKO-N); ANAM SEMICONDUCTOR LTD (ANAM-N); ANAM IND CO LTD (ANAM-N)
Inventor: HUH Y; SIM I; HEO Y W; SHIM I K
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5708567	A	19980113	US 96748937	A	19961113	199809	B
KR 97030690	A	19970626	KR 9541438	A	19951115	199828	
JP 10308466	A	19981117	JP 96182798	A	19960624	199905	
KR 201380	B1	19990615	KR 9541438	A	19951115	200060	

Abstract (Basic): US 5708567 A

A **ball grid** array (**BGA**) semiconductor **package** comprises a semiconductor chip (30) mounted on one side of a printed **circuit board** (PCB) (20). The PCB has a chip mounting die paddle (21) with an extension outside the **package**, a wire (31) connects a chip bond pad to a PCB trace (24) and a protective **encapsulant** (32) surrounds the chip and wire. A **ring**-type **heat sink** (10) is attached to the paddle extension and surrounds the **encapsulant** and many **solder balls** (40) welded to the other side of the PCB act as input and output terminals.

USE - In **ball grid** array semiconductor **packages** for use in multi-pin devices, VLSI and microprocessors

ADVANTAGE - The heat-dissipating area of the chip bottom is enlarged by the high thermal conductivity **heat sink**; plated through holes enhance the heat loss.

26/3,AB/18 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010916033
WPI Acc No: 1996-412984/199641
XRPX Acc No: N96-347614
Thermally and electrically enhanced **solder ball grid** IC

package for mounting on PCB - uses bonding pads with **solder ball grid** mounted on bottom surface and has IC mounted on **heat sink** and ground plane on the top surface

Patent Assignee: INTEL CORP (ITLC)
Inventor: BANERJEE K; MALLIK D; SETH A; SETH A K
Number of Countries: 071 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9627280	A1	19960906	WO 96US2000	A	19960215	199641	B
US 5557502	A	19960917	US 95399162	A	19950302	199643	
AU 9649241	A	19960918	AU 9649241	A	19960215	199701	
GB 2314458	A	19971224	WO 96US2000	A	19960215	199803	
			GB 9717189	A	19970814		

Abstract (Basic): WO 9627280 A

The IC **package** (10) has internal bonding pads (46) located on bonding shelves and coupled to internal power and ground planes (20, 24, 28) by conductive strips (52) that extend along the edges of the shelves. The bonding pads are coupled to an IC (12) that is mounted to a **heat sink** (54) attached to the top surface of the **package**. The **heat sink** functions as both a ground plane and a thermal sink for the IC. Capacitors (62) are coupled to the internal routing of the **package** to reduce the electrical noise of the signals provided to the IC and multiple power planes are dedicated to different voltage levels. The bonding and conductive planes are coupled to landing pads located on the bottom surface of the **package** and attached to the landing **pads** are **solder balls** (68) which can be soldered to an external PCB.

ADVANTAGE - ADVANTAGE - Reduces electrical noise and allows multiple voltage levels to be applied to the IC

Dwg.1/7

26/3,AB/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010573449
WPI Acc No: 1996-070402/199608
XRPX Acc No: N96-059096

Ball grid array **package** for integrated circuit - has **ball grid** array Vss plane between upper and lower traces with upper and lower Vss traces on outer periphery of vias electrically and thermally coupled to Vss plane to upper and lower Vas traces

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: SELNA E
Number of Countries: 007 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 692823	A1	19960117	EP 95110698	A	19950708	199608	B
JP 8172141	A	19960702	JP 95199228	A	19950711	199636	
US 5640048	A	19970617	US 94273331	A	19940711	199730	
			US 96718220	A	19960920		

Abstract (Equivalent): US 5640048 A

A **ball grid** array (''**BGA**'') **package** for an integrated circuit (''IC'') having improved **BGA package** thermal and electrical characteristics, comprising:

upper layer **BGA package** traces including a Vss trace, a Vdd trace, and a signal trace;

lower layer **BGA package** traces at least a portion of which traces are in vertical alignment with a corresponding one of said upper layer **BGA package** traces;

wherein regions of said lower layer **BGA package** traces are solderable to **solder balls** used to **solder** said **BGA package** to an underlying system printed **circuit board**;

BGA core material disposed between said upper and lower layer **BGA package** traces;

vias including a unitary-construction Vss via coupling said upper layer **BGA** Vss trace to a corresponding lower layer **BGA** Vss trace, a unitary-construction Vdd via coupling said upper layer **BGA** Vdd trace to a corresponding lower layer **BGA** Vdd trace, and a unitary-construction signal via coupling a said upper layer **BGA** signal trace to a corresponding lower layer **BGA** signal trace; and

a **BGA** Vss plane, disposed intermediate said upper and lower layer **BGA package** traces and making electrical contact with said Vss via.

26/3,AB/20 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06691824
SEMICONDUCTOR DEVICE

PUB. NO.: 2000-277654 [JP 2000277654 A]
PUBLISHED: October 06, 2000 (20001006)
INVENTOR(s): KUROSHIMA YUTAKA
KITAHARA MASARU
APPLICANT(s): KOKUSAI ELECTRIC CO LTD
APPL. NO.: 11-081584 [JP 9981584]
FILED: March 25, 1999 (19990325)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device, in which mechanical strength after the mounting of a **ball grid** array **package** on a print **circuit board** is improved.

SOLUTION: This semiconductor device is provided with a **ball grid** array **package** 11, in which plural **solder balls** 13 are arranged on the back face side of an **interposer** 16 in which a semiconductor chip is formed to be resin-sealed and a print **circuit board** 19 on which the **ball grid** array **package** 11 is mounted. Plural through-holes 21 and 21' are formed at the edge parts of the **ball grid** array **package** 11 and the print **circuit board** 19, and a fixing means is inserted into the through-holes 21 and 21' to be fixed.

? T S35/3,AB/1-4

35/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014227536
WPI Acc No: 2002-048234/200206
XRAM Acc No: C02-013427
XRPX Acc No: N02-035628
Manufacture of **chip**-sized semiconductor **package**, e.g. **ball grid** array, involves mounting on **chip** an insulative substrate having thermal coefficient of expansion closely matching that of the **chip**
Patent Assignee: AMKOR TECHNOLOGY INC (AMKO-N)
Inventor: GLENN T P; HOLLAWAY R D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6291884	B1	20010918	US 99437013	A	19991109	200206	B

Abstract (Basic): US 6291884 B1
Abstract (Basic):
NOVELTY - A **chip**-sized semiconductor **package** is made by mounting an insulative substrate (126) on the top surface of the **chip** (104). The rigid substrate has a thermal coefficient of expansion (TCE) equal to the TCE of the **chip** +/-2.5 ppm/degreesC.
DETAILED DESCRIPTION - Manufacture of **chip**-sized semiconductor **package** from a **chip** having contacts involves:
(a) mounting an insulative substrate on the top surface of the **chip**;
(b) electrically connecting first terminals of the conductors on the substrate to the contacts on the **chip**; and
(c) **encapsulating** the contacts on the **chip**, the first terminals on the substrate, and the conductive connectors with a protective **encapsulant**.
The rigid substrate has a thermal coefficient of expansion (TCE) equal to the TCE of the **chip** +/-2.5 ppm/degreesC.
An INDEPENDENT CLAIM is also included for a **chip**-size semiconductor **package** including a semiconductor **chip**, an insulative substrate, conductors, conductive connectors, and a protective layer of **encapsulant**.
USE - For producing surface-mounting, **chip**-size **ball grid** array (CS-**BGA**), land grid array, and lead-less **chip** carrier semiconductor **packages**.
ADVANTAGE - The method reduces manufacturing costs of the **packages** relative to that of individually **packaged chips**. It eliminates the need for a silicone **interposer** between the substrate and the **chip** otherwise necessary to prevent stress-related problems caused by the difference in the respective thermal expansion and contraction of the **chip** and substrate with changes in temperature. This, further reduces the cost of the **packages**, improves heat transfer from the **chips**, and results in a **package** that is free of thermal-induced stresses.

35/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014051191
WPI Acc No: 2001-535404/200159
XRAM Acc No: C01-159403
XRPX Acc No: N01-397536
Film **ball grid** array (**BGA**) **package** has dam provided between **chip** attaching area and **chip** connection pads in flexible film substrate
Patent Assignee: ADVANCED SEMICONDUCTOR ENG INC (ADSE-N)
Inventor: HSU K; LEE S; TAO S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010010947	A1	20010802	US 99444364	A	19991122	200159 B
			US 2001783983	A	20010216	

Priority Applications (No Type Date): US 99444364 A 19991122; US 2001783983 A 20010216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010010947	A1		7	H01L-021/44	Div ex application US 99444364

Abstract (Basic): US 20010010947 A1
Abstract (Basic):

NOVELTY - Upper surface of a flexible film (220a) in a flexible film substrate (220) has a **chip** attaching area with **chip** connection **pads** (220c). **Bonding pads** of a semiconductor **chip** (210) are electrically connected to associated pads (220c). A **package** (240) is formed on the semiconductor **chip** and upper surface of substrate. A dam (220f) is provided in flexible film between **chip** attaching area and pads.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) flexible film substrate; and

(b) flexible film substrate manufacture.

USE - Film **ball grid** array (**BGA**) **packages**.

ADVANTAGE - Bleeding of non-conductive adhesive to contaminate the **chip** connection pads is prevented by providing the dam in the flexible film substrate. The flexible film substrate has **stiffener** formed for increasing the rigidity of the flexible film substrate.

35/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014044571
WPI Acc No: 2001-528784/200158
XRPX Acc No: N01-392409
Heat sink fixing method on substrate for **ball grid** array **package**, involves interconnecting ground **ring** on substrate to ground pads on which legs of **heat sink** is mounted
Patent Assignee: ST ASSEMBLY TEST SERVICES PTE LTD (STAS-N)
Inventor: FERNANDEZ E A; GUAN C S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

US 6278613 B1 20010821 US 2000670380 A 20000927 200158 B

Abstract (Basic): US 6278613 B1
Abstract (Basic):
NOVELTY - Interconnect metal having conductive **rings** is provided to the central area of a substrate on which a semiconductor device is mounted. A ground **ring** (76) and a power **ring** (78) surround the central **conductive ring**. Ground **pads** (72) around the **conductive ring**, contact support legs of a **heat sink**, and are connected to the ground **ring** by interconnection traces.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor **package**.
USE - For semiconductor **packages** such as **ball grid** array (**BGA**) **package**, flip-**chip** **package**.
ADVANTAGE - **Package** design flexibility increases by eliminating the direct ground pad connections to ground **ring**, and by connecting **heat sink** to copper pads.
DESCRIPTION OF DRAWING(S) - The figure shows the top view of the heat conducting copper pads connected to a ground **ring** of the **package**.

35/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013990663
WPI Acc No: 2001-474878/200151
Related WPI Acc No: 2001-464390
XRAM Acc No: C01-142314
XRPX Acc No: N01-351462
Application of thermoplastic polymer to semiconductor component, e.g. printed circuit board, to form bonding layers involves applying dispersion comprising thermoplastic particles and liquid medium
Patent Assignee: MICRO TECHNOLOGY INC (MICR-N)
Inventor: COBBLEY C A; JIANG T; VANNORTWICK J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6238223	B1	20010529	US 97915211	A	19970820	200151	B

Abstract (Basic): US 6238223 B1
Abstract (Basic):
NOVELTY - A thermoplastic polymer is applied to a semiconductor component by providing a dispersion comprising thermoplastic particles and liquid medium. The dispersion is applied on the surface of semiconductor component and then dried.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the formation of an array of conductive thermoplastic deposits on molded body surface of **integrated circuit package**.
USE - For applying thermoplastic polymer to semiconductor component e.g. **wafers**, **dies**, leadframe, lead fingers, **wire** **bonds** and printed circuit board or flip **chip** mounted on printed circuit board to form **bonding** layers (15), **pads** or bumps. It is useful in surface mount attachment of devices (10) to e.g. printed circuit boards (14), **chip**-on board (COB), lead on

chip (LOC), direct **chip** attach (DCA) and **ball grid** arrays (**BGA**).

35/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013750590
WPI Acc No: 2001-234819/200124
XRAM Acc No: C01-070276
XRPX Acc No: N01-167934
Semiconductor device **package**, e.g. **ball grid** array type **package**, uses pieces of adhesive film to attach a semiconductor **die** to an **interposer** having interconnects
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: JIANG T
Number of Countries: 090 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200109939	A1	20010208	WO 2000US20583	A	20000728	200124	B
AU 200063879	A	20010219	AU 200063879	A	20000728	200129	

Abstract (Basic): WO 200109939 A1
Abstract (Basic):
NOVELTY - A semiconductor device **package** consists of a semiconductor **die**; an electrically conductive external terminal; an **interposer**; and pieces of adhesive film disposed between the semiconductor **die** and the **interposer** to adhere the semiconductor **die** to the **die**-attach surface of the **interposer**.
DETAILED DESCRIPTION - A semiconductor device **package** comprises a semiconductor **die** (12); an electrically conductive external terminal; an **interposer** (16); and pieces of adhesive film. The semiconductor **die** has a first surface where an **integrated circuit** and an electrically **conductive** bond **pad** (14) are fabricated. The **interposer** has a **die**-attach surface, an external surface opposite the **die** -attach surface, and an electrically conductive interconnect (18) electrically coupling the bond pad to the external terminal. It is disposed between the semiconductor **die** and the external terminal. The pieces of adhesive film are disposed between the semiconductor **die** and the **interposer** to adhere the semiconductor **die** to the **die**-attach surface of the **interposer**. An INDEPENDENT CLAIM is also included for a method of **packaging** a semiconductor device by laminating pieces of adhesive film to an **interposer**, attaching the semiconductor **die** to the **interposer**, and bonding the electrically conductive interconnect to the electrically **conductive** bond **pad**.

35/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013279330
WPI Acc No: 2000-451265/200039
XRPX Acc No: N00-335934
Ball grid array semiconductor **die** test for **BGA** characteristics evaluation, involves assembling **die**, test

interposer and carrier substrate so that bond **pad**, **conductive** via and terminal electrically communicate
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: BARRETT K E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6081429	A	20000627	US 99234242	A	19990120	200039	B

Abstract (Basic): US 6081429 A
Abstract (Basic):

NOVELTY - An electrically optimized carrier substrate (40) and test **interposer** (10) with an electrically conductive via (18) and test pad (22), are selected. The semiconductor **die** (30), test **interposer** and the substrate are assembled so that a bond pad (32), via and a terminal electrically communicate. Electrical characteristic of the **die** is determined by probing test pad, during assembling with the substrate.

DETAILED DESCRIPTION - The carrier substrate including one terminal (42) positioned corresponding to one bond pad of the semiconductor **die** is selected. The test **interposer** including one electrically conductive via corresponding to one bond pad and the terminal, and test pad disposed at periphery of test **interposer**, is selected. The electrical characteristic of semiconductor **die** is determined by probing test pad, during assembling of semiconductor **die**, test **interposer** and carrier substrate.

USE - For evaluating characteristics of **ball grid** array **package** or **BGA** semiconductor **die**.

ADVANTAGE - Since the test **interposer** is of small size, it is assembled with **BGA** semiconductor **die** and carrier substrate, without increasing surface area consumed on the carrier substrate relative to surface area consumed by **BGA** semiconductor **die** alone, and without significantly interfering with signals transmitted through semiconductor **die** or through substrate.

35/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012889436
WPI Acc No: 2000-061270/200005
Related WPI Acc No: 1996-277031; 1997-013963; 1999-142143; 2000-646774
XRPX Acc No: N00-047971
Land grid array carrier for mounting multi **chip package**
Patent Assignee: INTEL CORP (ITLC)
Inventor: BROWNELL M P; PHILLIPS P T; SAMARAS W A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5991161	A	19991123	US 97993793	A	19971219	200005	B

Abstract (Basic): US 5991161 A
Abstract (Basic):

NOVELTY - The semiconductor **dies** (16) and passive components (18) are coupled to top surface (13) of **interposer** (12) made of organic material whose bottom surface (24) is provided with

conductive pads (26). The **conductive pads** which are electrically coupled to components on top surface of **interposer** are attached to solder balls (30).

DETAILED DESCRIPTION - The **interposer** is coupled to other devices through pins provided in selected **conductive pads** arranged in array of rows and columns.

USE - In land grid array carrier for mounting multi **chip package** e.g. **ball grid** array **package**.

ADVANTAGE - The **conductive pads** that are coupled to components on top surface only have solder balls attached to them which enhances design flexibility and reduces cost.

DESCRIPTION OF DRAWING(S) - The figure shows the end view of electrical coupling arrangement in land grid array carrier.

35/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012867068
WPI Acc No: 2000-038901/200003
XRAM Acc No: C00-010028
XRPX Acc No: N00-029330
Packaging component for **integrated circuit die** used in printed circuit boards
Patent Assignee: MINNESOTA MINING & MFG CO (MINN); 3M INNOVATIVE PROPERTIES CO (MINN)
Inventor: HARVEY P M; PLEPYS A R
Number of Countries: 024 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9957764	A1	19991111	WO 99US7087	A	19990331	200003	B
US 6140707	A	20001031	US 9874126	A	19980507	200057	
EP 1082762	A1	20010314	EP 99914308	A	19990331	200116	
			WO 99US7087	A	19990331		

Abstract (Basic): WO 9957764 A1
Abstract (Basic):

NOVELTY - The **packaging** component comprises flexible dielectric tape (60) whose upper surface has selected pattern of conductive traces (62) made of **die** attachment pads (56) and **ball- grid**-array (**BGA**) attachment pads (64) and lower surface has openings for exposing **BGA** attachment **pads**. **Conductive** traces are covered by dielectric adhesive layer (58) attached with **stiffener** (52) having a window.

DETAILED DESCRIPTION - Openings in the adhesive expose **die** attachment pads.

INDEPENDENT CLAIMS are included for the following: (i) A **packaged integrated circuit** which has **packaging** component **containing BGA** solder balls (30) attached to **BGA** attachment pads through the opening and an **integrated circuit die** (32) disposed within the window formed in the **stiffener**. (ii) Manufacture of **packaging** component. The **stiffener** is laminated on dielectric adhesive layer using an adhesive. A window is formed in the **stiffener** by etching to expose a portion of the tape and adhesive overlying the **die** attachment pads. The adhesive overlying **die** attachment pads are then removed.

USE - The **packaging** component is used for flip-**chip integrated circuit die** used in printed circ

35/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012850133
WPI Acc No: 2000-021965/200002
XRAM Acc No: C00-005243
XRPX Acc No: N00-016239
Semiconductor device having a flip-**chip** bump structure
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: BEDDINGFIELD S C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5977632	A	19991102	US 9817562	A	19980202	200002	B

Abstract (Basic): US 5977632 A
Abstract (Basic):
NOVELTY - A semiconductor device having a flip-**chip** **bump** structure includes a **conductive** bond **pad**, a polyimide toroid coated with a conductive layer and a **conductive** **bump** contacting the bond pad through the toroid.
DETAILED DESCRIPTION - The toroid is preferably an annular **ring** of polyimide having a flat top and covered with a layer of conductive material, preferably formed of first and second metal layers. A passivation layer is provided between the toroid and the substrate. A second similar polyimide toroid structure is preferably provided spaced from the first.
USE - As part of a semiconductor device **package**, especially a **Ball Grid** Array **package** or a **Chip** Scale **package**, which includes underfill material applied adjacent the bump structure (claimed).
ADVANTAGE - The use of a polyimide toroidal structure as opposed to a polyimide layer, overcomes prior art problems of delamination between the polyimide and underfill material.
DESCRIPTION OF DRAWING(S) - The drawings show a completed bump interconnect structure of the invention.

35/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012421935
WPI Acc No: 1999-228043/199919
XRAM Acc No: C99-067032
XRPX Acc No: N99-168654
Transfer flat type **ball grid** array method for making a **packaging** substrate - forms circuit on one side of substrate only by selective electroplating
Patent Assignee: COMPEQ MFG CO LTD (COMP-N)
Inventor: LIN T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5884396	A	19990323	US 97846857	A	19970501	199919	B

Abstract (Basic): US 5884396 A
NOVELTY - A **packaging** substrate is manufactured by a transfer flat type **ball grid** array method which electroplates a circuit pattern on one side of a copper plate only, laminates a dielectric layer and a metal plate and then removes the copper plate and attaches a **die** into the laminate.
DETAILED DESCRIPTION - A transfer flat type **ball grid** array method of manufacturing a **packaging** substrate comprises selectively applying a photoresist onto a copper plate and then electroplating to give a raised circuit pattern (12). The photoresist is removed and a dielectric layer and a metal plate laminated and the copper plate etched away to expose the circuit pattern. Solder resist is selectively applied, a cavity opening for **die** attachment in the laminate defined, a **heat sink** attached and dam **rings** (34) formed on the laminate which is protected by a side mold layer (33). A **die** (40) is attached to the cavity , gold **wires** (41) **bonded** between the **die pads** and **wire bonding pads** and the cavity opening then **encapsulated** (50). Solder balls (60) are then attached by soldering on the bottom of the laminate.
USE - As a flat transfer type **ball grid** array method for **packaging** substrates (claimed)
ADVANTAGE - Fine circuitry is formed, waste reduced, heat dissipation increased and yield improved.

35/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012376935
WPI Acc No: 1999-183042/199916
XRPX Acc No: N99-134455
Integrated circuit package e.g. **ball grid** array (**BGA**) type
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: ORCUTT J W
Number of Countries: 030 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

EP 903780	A2	19990324	EP 98116369	A	19980828	199916	B
JP 11251355	A	19990917	JP 98284810	A	19980921	199949	
SG 68074	A1	19991019	SG 983577	A	19980907	199950	
KR 99029932	A	19990426	KR 9838673	A	19980918	200028	
US 6194786	B1	20010227	US 9759539	A	19970919	200114	
			US 98153745	A	19980915		
TW 436949	A	20010528	TW 98115383	A	19980916	200172	

Abstract (Basic): EP 903780 A2
Abstract (Basic):
NOVELTY - The **package** has a **die** cavity (12) in a substrate (11). There are signal traces (20) on the substrate and at least one region isolated from the traces positioned between the traces and bond **pads** (21). An electrically **conductive** ball spacer (24) is positioned on and above the traces. A bond wire (19) connects the **die** and part of the spacer remote from the signal trace. The bond wire crosses and is electrically isolated from the region.
DETAILED DESCRIPTION - An independent claim is included for a method of forming a wire bonding a semiconductor **die** to a substrate.
USE - For **ball grid** array (**BGA**) and pin grid array (PGA) **integrated circuit packages**.
ADVANTAGE - Provides reliable wire clearance for bond wires that pass over power and ground **rings**.
DESCRIPTION OF DRAWING(S) - The drawing shows a close up sectional view of a **package** according to the invention.

35/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012335986
WPI Acc No: 1999-142093/199912
Related WPI Acc No: 2001-535495
XRPX Acc No: N99-103223
Heat sink for semiconductor **chip** of **BGA**, PGA, TAB, SLICC type
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: AKRAM S; WARK J M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5866953	A	19990202	US 96653030	A	19960524	199912	B

Abstract (Basic): US 5866953 A
Abstract (Basic):
NOVELTY - A barrier glob top (424) surrounds the edge of the **chip** and forms a surrounding wall that defines a recess (426) on the **chip**. A heat dissipating glob top (428) is in the recess so that the **chip** is sealed by the barrier and the glob top.
DETAILED DESCRIPTION - The semiconductor **chip** (402) is mounted on a substrate (416) with its bond pads (404) electrically connected to the respective bonding pads (412) on the mounting surface of the substrate by **conductive pads** (410). An INDEPENDENT CLAIM is also included for a semiconductor assembly manufacturing method.
USE - For a semiconductor **chip** of **BGA**, PGA, TAB or

SLICC type.
ADVANTAGE - Reduces the difference in thermal coefficient of expansion and potential of separation between the barrier and the heat dissipating glob top. Seals the semiconductor **chip** completely and prevents it from moisture and external contamination.
DESCRIPTION OF DRAWING(S) - The figure shows a side cross sectional view of an **encapsulated** semiconductor **chip**.

35/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012143341
WPI Acc No: 1998-560253/199848
XRAM Acc No: C98-167831
XRPX Acc No: N98-436911
Ball grid array (**BGA**) **package** for **integrated circuits** used in e.g. mobile telephones - has a metal **heat sink covered** in an insulating sheet including conductive traces, with a central hole into which is mounted the device
Patent Assignee: HYUNDAI ELECTRONICS IND CO LTD (HYUN-N)
Inventor: CHOI K H; JEONG T S; LEE T K; PARK J S; RYU K T; YOUN H S; CHOI K ; JEONG T; LEE T; PARK J; RYU K; YOUN H; CHOI G H; CHUNG T S; LEE T G; RYOO G T; YOON H S
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2325340	A	19981118	GB 986078	A	19980320	199848	B
DE 19821715	A1	19990128	DE 1021715	A	19980514	199910	
CN 1199927	A	19981125	CN 98107932	A	19980506	199915	
JP 11045956	A	19990216	JP 98100428	A	19980327	199917	
KR 98083733	A	19981205	KR 9719144	A	19970517	200007	
KR 98083734	A	19981205	KR 9719145	A	19970517	200007	
US 6060778	A	20000509	US 9860981	A	19980415	200030	

Abstract (Basic): GB 2325340 A
An **integrated circuit package** comprises an interconnection substrate (50) with a conductive trace layer on each side. A first side (50b) is bonded to a thermally conductive layer (35). The substrate and thermally conductive layer are essentially square, with a hole (36) in the centre. An **integrated circuit** device (40) is located in the central hole and connected to bond **pads** on the **conductive** traces on the second side of the insulating substrate before being **encapsulated** (42) and fixed in the hole. Solder balls connect to the conductive traces on the second side of the insulating layer. Preferably the first side of the insulating layer has an epoxy or polyimide layer around its periphery. The thermally conductive layer is made from aluminium silver or copper.
USE - The **ball grid** array **package** is used for **integrated circuit** devices used in portable equipment such as mobile telephones, pocket computers etc.
ADVANTAGE - The device **package** is low-profile, light, cheap to make and has excellent heat dissipation properties.

35/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010916033
WPI Acc No: 1996-412984/199641
XRPX Acc No: N96-347614
Thermally and electrically enhanced solder **ball grid IC package** for mounting on PCB - uses bonding pads with solder **ball grid** mounted on bottom surface and has **IC** mounted on **heat sink** and ground plane on the top surface
Patent Assignee: INTEL CORP (ITLC)
Inventor: BANERJEE K; MALLIK D; SETH A; SETH A K
Number of Countries: 071 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9627280	A1	19960906	WO 96US2000	A	19960215	199641	B
US 5557502	A	19960917	US 95399162	A	19950302	199643	
AU 9649241	A	19960918	AU 9649241	A	19960215	199701	
GB 2314458	A	19971224	WO 96US2000	A	19960215	199803	
			GB 9717189	A	19970814		

Abstract (Basic): WO 9627280 A
The **IC package** (10) has internal bonding pads (46) located on bonding shelves and coupled to internal power and ground planes (20, 24, 28) by conductive strips (52) that extend along the edges of the shelves. The bonding pads are coupled to an **IC** (12) that is mounted to a **heat sink** (54) attached to the top surface of the **package**. The **heat sink** functions as both a ground plane and a thermal sink for the **IC**. Capacitors (62) are coupled to the internal routing of the **package** to reduce the electrical noise of the signals provided to the **IC** and multiple power planes are dedicated to different voltage levels. The bonding and conductive planes are coupled to landing pads located on the bottom surface of the **package** and attached to the landing pads are solder balls (68) which can be soldered to an external PCB.
ADVANTAGE - ADVANTAGE - Reduces electrical noise and allows multiple voltage levels to be applied to the **IC**

35/3,AB/15 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06482833
SEMICONDUCTOR PLASTIC **PACKAGE**

PUB. NO.: 2000-068411 [JP 2000068411 A]
PUBLISHED: March 03, 2000 (20000303)
INVENTOR(s): TAKE MORIO
IKEGUCHI NOBUYUKI
KOBAYASHI TOSHIHIKO
APPLICANT(s): MITSUBISHI GAS CHEM CO INC
APPL. NO.: 10-250445 [JP 98250445]
FILED: August 20, 1998 (19980820)

ABSTRACT
PROBLEM TO BE SOLVED: To provide a semiconductor plastic **package** with superior connection between an inner-layer metal core and an outer layer metal foil, **heat radiation**, **heat** resistance, after moisture absorption, etc.

SOLUTION: In a semiconductor plastic **package** with a **ball**

grid array using both-sided truncated conical metal cores with both surfaces, truncated conical protrusions on the front surface and the rear surface are individually exposed between semiconductor **chip** mounted metal foils a and between metal foils for ball pads, respectively. After a desmearing treatment of the exposed metal surfaces, the entire surfaces are metal-plated and coated with a plating resist, excluding a semiconductor **chip** mounting part g, the **bonding pad** parts and ball pad parts. In the printed wiring board obtained by plating with a noble metal h, a metal core c and a through-hole f are insulated by a thermosetting resin composition such as multifunctional cyanate ester, etc. A semiconductor **chip** is fastened on one surface of the wiring board with a heat-conductive adhesive and the **chip**, **wires** and **bonding pads** are resin-sealed in this semiconductor plastic **package**.

35/3,AB/16 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06272978
SEMICONDUCTOR PLASTIC **PACKAGE**

PUB. NO.: 11-214566 [JP 11214566 A]
PUBLISHED: August 06, 1999 (19990806)
INVENTOR(s): TAKE MORIO
IKEGUCHI NOBUYUKI
YAMANE KOZO
APPLICANT(s): MITSUBISHI GAS CHEM CO INC
APPL. NO.: 10-011528 [JP 9811528]
FILED: January 23, 1998 (19980123)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a semiconductor plastic **package** whose **heat radiation** and **heat** resistance after moisture absorption or the like are excellent.

SOLUTION: This is a semiconductor plastic **package** of a **ball grid** array using a metal core print wiring board. One part of a metal core is exposed at one part of the front and back surfaces, and a semiconductor **chip** fixed on the exposed metal pat on the surface and the surrounding circuit conductor are connected by **wire bonding**. A front and back circuit insulated by a thermosetting resin composition with the metal core is conducted by a through-hole conductor insulated through the thermosetting resin composition with the metal core having a slit hole, and one or more through-holes are directly connected with the metallic core, and the semiconductor **chip**, **wire**, and **bonding pad** are resin sealed.

35/3,AB/17 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06272975
SEMICONDUCTOR PLASTIC **PACKAGE**

PUB. NO.: 11-214563 [JP 11214563 A]
PUBLISHED: August 06, 1999 (19990806)
INVENTOR(s): TAKE MORIO
IKEGUCHI NOBUYUKI
YAMANE KOZO
APPLICANT(s): MITSUBISHI GAS CHEM CO INC
APPL. NO.: 10-009568 [JP 989568]
FILED: January 21, 1998 (19980121)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a semiconductor plastic **package** whose **heat radiation** and **heat** resistance after moisture absorption or the like is excellent.

SOLUTION: This is a semiconductor plastic **package** of a **ball grid** array using a metal core print wiring board. One part of a metal core is exposed at one part of the front and back surfaces, and a semiconductor **chip** fixed on the exposed metal part on the surface and the surrounding circuit conductor are connected through **wire bonding** . A front and back circuit insulated through a thermosetting resin composition with the metal core is conducted by a through-hole conductor insulated through the thermosetting resin composition with the metal core having a slit hole, and the metal core exposed part on the back face is used for **heat radiation**, and the semiconductor **chip**, **wire**, and **bonding pad** are resin sealed.

35/3,AB/18 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

06272974
SEMICONDUCTOR PLASTIC **PACKAGE**

PUB. NO.: 11-214562 [JP 11214562 A]
PUBLISHED: August 06, 1999 (19990806)
INVENTOR(s): TAKE MORIO
IKEGUCHI NOBUYUKI
YAMANE KOZO
APPLICANT(s): MITSUBISHI GAS CHEM CO INC
APPL. NO.: 10-009567 [JP 989567]
FILED: January 21, 1998 (19980121)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a semiconductor plastic **package** whose **heat radiation** and **heat** resistance after moisture absorption or the like is excellent.

SOLUTION: This is a semiconductor plastic **package** of a **ball grid** array using a metallic core print wiring board. One part of a metallic core is exposed at one part of the front and back surfaces, and a semiconductor **chip** fixed on the exposed metallic part on the surface and the surrounding conductor are connected through **wire bonding** . A front and back circuit insulated through a thermosetting resin composition with the metallic core is conducted by a through-hole conductor insulated with the metallic core, and the metallic core exposed part on the back face is used for **heat radiation**, and the semiconductor **chip**, **wire**, and **bonding pad** are resin sealed. Thus, a semiconductor plastic **package** whose **heat radiation** and **heat** resistance after moisture absorption is excellent in a new structure suitable for mass productivity can be obtained.

35/3,AB/19 (Item 5 from file: 347)

06263104
SEMICONDUCTOR PLASTIC **PACKAGE**

PUB. NO.: 11-204685 [JP 11204685 A]
PUBLISHED: July 30, 1999 (19990730)
INVENTOR(s): TAKE MORIO
IKEGUCHI NOBUYUKI
YAMANE KOZO
APPLICANT(s): MITSUBISHI GAS CHEM CO INC
APPL. NO.: 10-004835 [JP 984835]
FILED: January 13, 1998 (19980113)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor plastic **package** having superior **heat radiation** performance and **heat** resistance after absorption of moisture.

SOLUTION: This semiconductor plastic **package** of **ball grid** array type uses a metal core printed wiring board, and metal core projections are exposed outside on a part of top and bottom surfaces. A semiconductor **chip** , fixed to the metal core projection on the top surface, is **wire-bonded** to a circuit conductor around the **chip** , and the circuits on the top and bottom surfaces are connected via a through-hole and **heat** is **radiated** from the metal core projection exposed on the bottom surface. At least a semiconductor **chip**, the wiring, and a **bonding pad** are **encapsulated** by resin. This semiconductor plastic **package** obtained has superior **heat radiation** performance and **heat** resistance after the absorption of moisture and is suitable for mass production.